EVALPFC2-ICE2PCS01

300W PFC Evaluation Board with CCM PFC controller ICE2PCS01

Power Management & Supply

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EVALPFC2-ICE2PCS01

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9&10	Capacitor CX1 size changed	

300W PFC Evaluation Board with CCM PFC controller ICE2PCS01 A N - P S 0 0 1 0
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1 Content

The evaluation board described here is a 300W power factor correction (PFC) circuit with 85~265VAC universal input and 393VDC fixed output. Boost converter topology is employed in this board. The continuous conduction mode (CCM) PFC controller **ICE2PCS01** is employed in this board to achieve the unity power factor. The switching frequency is programmable by external resistor at one pin. There are various protection features incorporated to ensure safe system operation conditions. The device has a unique soft-start function which limits the start up inrush current thus reducing the stress on the boost diode. To improve the efficiency, the third generation **CoolMOS™** is used as the power switch due to its lowest area specific Rdson. High voltage Silicon Carbide (SiC) Schottky diode **thinQ!™** is used as PFC boost diode. Because of its ideal reverse recovery behavior, SiC Schottky diode is extremely suitable for high frequency CCM PFC application.

2 Evaluation board

3 Technical specifications:

Input voltage	85VAC~265VAC
Input frequency	50Hz
Output voltage and current	393VDC, 0.75A
Output power	~ 300W
Efficiency	>90% at full load
Switching frequency	62.5kHz (with R8=76K)

4 Circuit Description

Line Input

The AC line input side comprises the input fuse F1 as over-current protection. The high frequency current ripple is filtered by R1, L1 and CX1. The choke L2, X2-capacitors CX1 and CX2 and Y1-capacitor CY1 and CY2 are used as radio interference suppressors. RT1 is placed in series to limit inrush current during each power on.

Power Stage – Boost Type PFC Converter

After the bridge rectifier BR1, there is a boost type PFC converter consisting of L3, Q1, D1 and C2. The third generation **CoolMOS™** is used as the power switch Q1. Due to its low Rdson, the small heat sink can fulfill the dissipation requirement. SiC Schottky diode **thinQ!™** is used for D1. As SiC Schottky diode does not show a reverse recovery behavior, the stress on the MOSFET will be reduced due to very low current spike during turn on transient. Simultaneously higher reliability of the entire system can be achieved. However, due to the poor pulse current capability of SiC Schottky diode, a standard diode D2 is necessary to bypass the high inrush current during each power on transient. Output capacitor C2 provides energy buffering to reduce the output voltage ripple (100Hz) to the acceptable level.

PWM control of Boost Converter

The PWM control is realized by 8-Pin CCM PFC IC **ICE2PCS01**. Unlike the conventional PFC controller, **ICE2PCS01** does not need direct sine wave reference signal. The switching frequency is fixed and programmed by R8. There are two control loops in the circuit, voltage loop and current loop. The output voltage is sensed by the voltage divider of R5A, R5B, R6A and R6B and sent to internal error amplifier. The output of error amplifier is used to control current in the inner current loop. The compensation network C4, C5, R7 constitutes the external circuitry of the error amplifier. This circuitry allows the feedback to be matched to various load conditions, thereby providing stable control. In order not to make the response for 100Hz ripple, the voltage loop compensation is implemented with low bandwidth. The inner loop, current control loop, is implemented with average current mode strategy. The instant current is adjusted to be proportional to both of MOSFET off duty D_{OFF} and the error amplifier output voltage of voltage loop. The current is sensed by shunt resistors R2, R2A and R2B and fed into IC through R9. The current sense signal is averaged by an internal operating amplifier and then processed in the PWM generator which drives the gate drive. The averaging is realized by charging and discharging an external capacitor C7.

The IC supply is provided by external voltage source and filtered and buffered by C8 and C9. The IC output gate driver is a fast totem pole gate drive. It has an in-built cross conduction current protection and a Zener diode to protect the external transistor switch against undesirable over voltages. The gate drive resistor R4 is selected to limit and gate pulse current and drive MOSFET for fast switching.

5 Circuit Operation

Soft Start

When Vcc pin is higher than turn-on threshold, typical 11V, PFC is going to start. The unique soft start is integrated. Input current keeps sinusoidal and is increasing gradually until output voltage reaches

75% of rating. Because the peak current limit is not activated, the boost diode is not stressed with large diode duty cycle under high current.

Enhanced Dynamic Response

Due to inherent low bandwidth of PFC dynamic, in case of load jump, regulation circuit can not response fast enough and it will lead to large output voltage overshoot or drop. To solve this problem in PFC application, enhance dynamic response is implemented in the IC. Whenever output voltage exceeds by ±5%, it will bypass the slow compensation operating amplifier and act on the nonlinear gain block to affect the duty cycle directly. The output voltage can be recovered in a short time.

Protection Features

a. Open loop protection (OLP) / Mains under voltage protection

The open loop protection is available for this IC to safe-guard the output. Whenever V_{SENSE} voltage falls below 0.6V, or equivalently V_{OUT} falls below 20% of its rated value, it indicates an open loop condition (i.e. VSENSE pin not connected). In this case, most of the blocks within the IC will be shutdown. It is implemented using a comparator with a threshold of 0.6V. Insufficient input voltage V_{IN} will also trigger this protection.

b. Output over-voltage protection

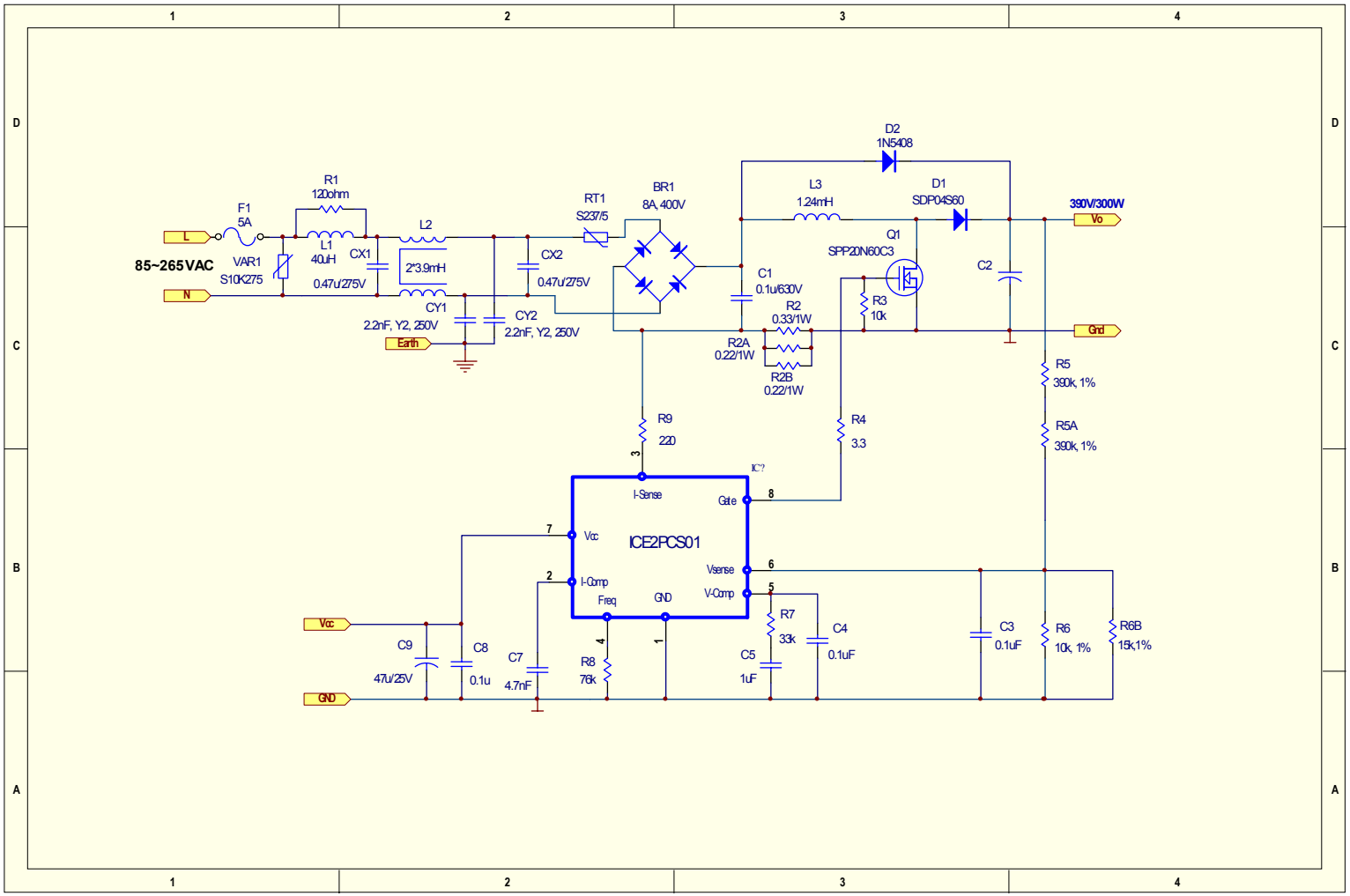
Output over-voltage protection is also available by the same integrated blocks of enhanced dynamic response. Whenever V_{OUT} exceeds the rated value by 5%, the over-voltage protection OVP is active. This is implemented by sensing the voltage at pin V_{SENSE} with respect to a reference voltage of 3.15V. A V_{SENSE} voltage higher than 3.15V will immediately reduce the output duty cycle even down to zero, bypassing the normal voltage loop control. This results in a lower input power and the output voltage V_{OUT} is reduced.

c. Soft over current control (SOC) and peak current limit
When the amplitude of current sense voltage reaches 0.68V, Soft Over Current Control (SOC) is activated. This is a soft control does not directly switch off the gate drive but acts on the internal blocks to result in a reduced PWM duty cycle.

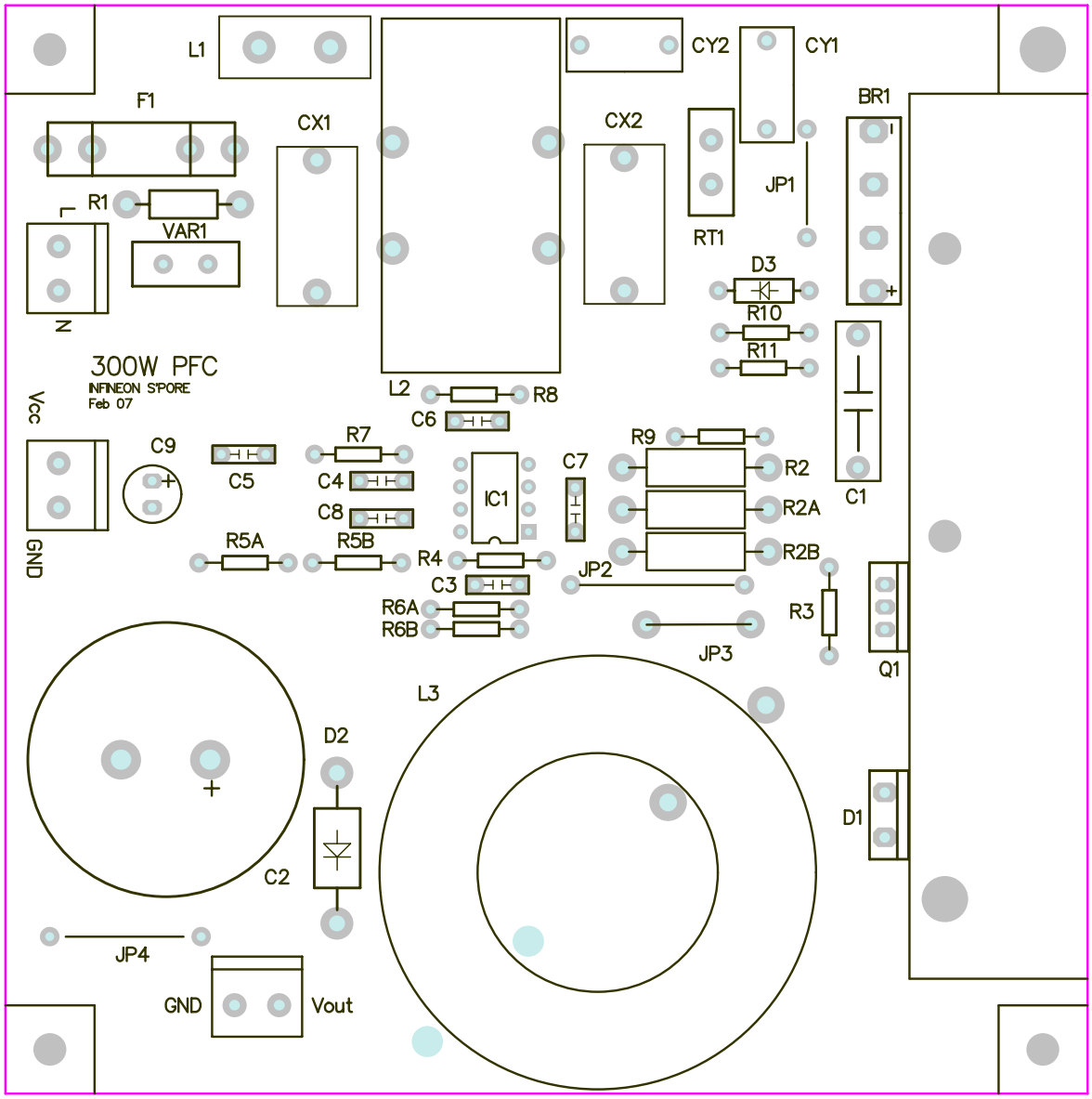
The IC also provides a cycle by cycle peak current limitation (PCL). It is active when the voltage at current sense voltage reaches -1.04V. The gate output is immediately off after 300ns blanking time.

d. IC supply under voltage lock out
When VCC voltage is below the under voltage lockout threshold VCCUVLO, typical 11V, IC is off the gate drive is internally pull low to maintain the off state. The current consumption is down to 200uA only.

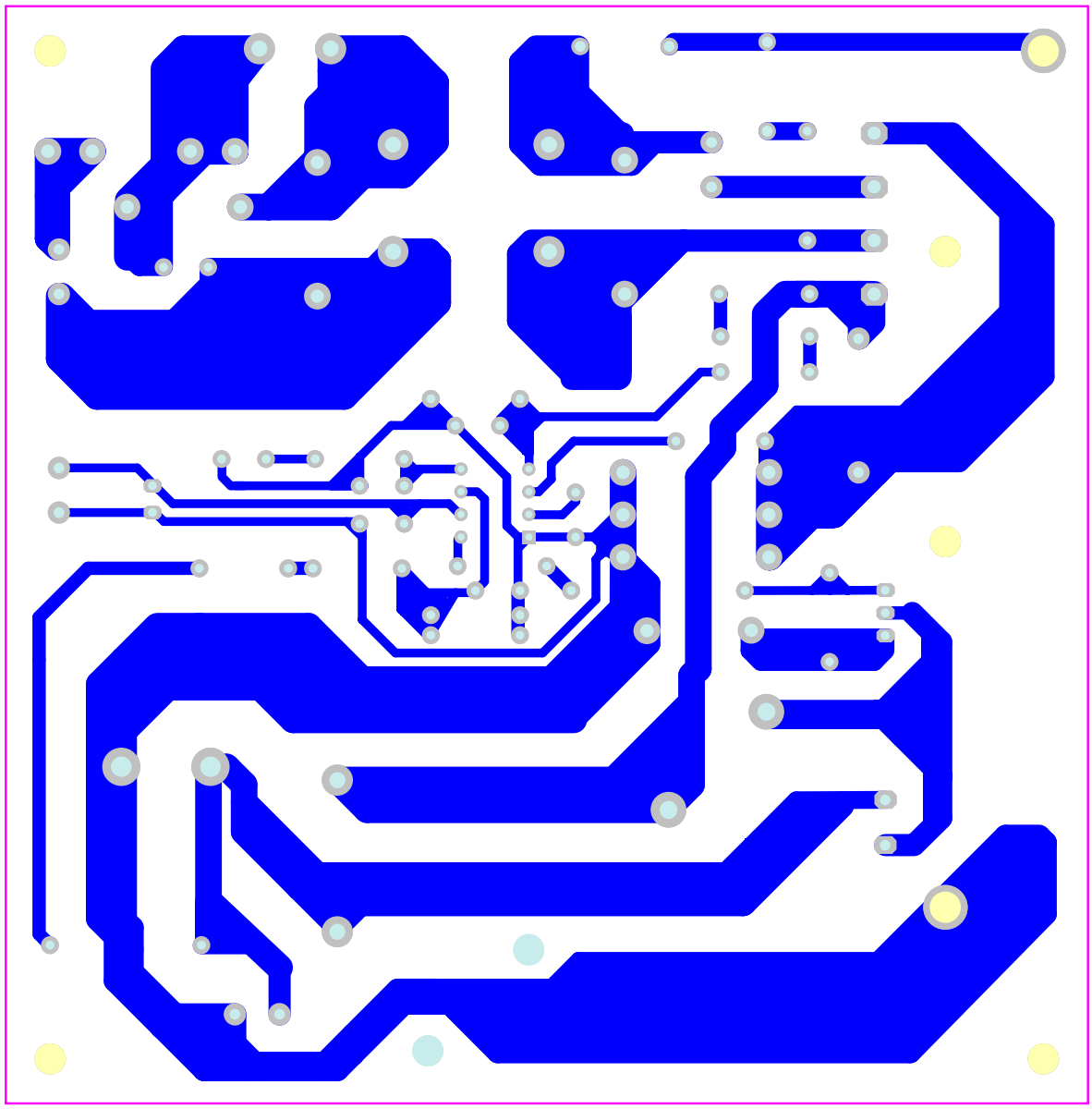
6 Circuit Diagram



7 PCB layout top layer



8 PCB layout Bottom:



9 Component List:

Designator	Part Type	Description	Manufacturer / Part No.
BR1	8A, 400V	Bridge Rectifier	Vishay / KBU8G
C1	0.1uF/630V	Ceramic Cap	Epcos / B32652A6104J
C2	220uF/450V	Electrolytic Cap	Epcos / B43304C5227M
C3	0.1uF/50V	Ceramic Cap	Murata / RPER71H104K2K1A03B
C4	0.1uF/50V	Ceramic Cap	Murata / RPER71H104K2K1A03B
C5	1uF/50V	Ceramic Cap	
C7	4.7nF/50V	Ceramic Cap	
C8	0.1uF/50V	Ceramic Cap	Murata / RPER71H104K2K1A03B
C9	47uF/25V	Electrolytic Cap	
CX1	0.47uF, X1, 305V	Ceramic Cap	Epcos / B32922C3474M
CX2	0.47uF, X1, 305V	Ceramic Cap	Epcos / B32922C3474M
CY1	2.2nF, Y2, 250V	Ceramic Cap	Epcos / B81123C1222M000
CY2	2.2nF, Y2, 250V	Ceramic Cap	Epcos / B81123C1222M000
		Connector	
D1	SDT04S60	Diode	
D2	1N5408	Diode	Vishay / 1N5408
F1	5A	Fuse	
		Fuse Holder	
IC1	ICE2PCS01		Infineon
JP1	12.5mm, Φ0.7mm	Jumper	
JP2	20mm, Φ0.7mm	Jumper	
JP3	12mm, Φ1.2mm	Jumper	
JP4	17.5mm, Φ0.7mm	Jumper	
L1*	Shorted		
L2	2*3.9mH	CM Choke	Epcos / B82725J2602N20
L3	1.24mH	Choke	
Q1	SPP20N60C3	Power MOSFET	Infineon
		Heat Sink	
		TO220 Clip	
		TO247 Clip	
		TO220 Isolation Pad	
		3mm Screw	
R2	0.33/1W, 5%	Metal Film Resistor	
R2A	0.22/1W, 5%	Metal Film Resistor	
R2B	0.22/1W, 5%	Metal Film Resistor	
R3	10k/0.25W, 5%	Carbon Film Resistor	
R4	3.3/0.25W, 5%	Carbon Film Resistor	
R5A	390k/0.25W, 1%	Carbon Film Resistor	
R5B	390k/0.25W, 1%	Carbon Film Resistor	
R6A	10k/0.25W, 1%	Carbon Film Resistor	
R6B	15k/0.25W, 1%	Carbon Film Resistor	
R7	33k/0.25W, 5%	Carbon Film Resistor	
R8	75k/0.25W, 1%	Carbon Film Resistor	
R9	220/0.25W, 5%	Carbon Film Resistor	
RT1	S237/5	NTC Thermistor	Epcos / B57237S509M
VAR1	S10K275	Varistor	Epcos / B72210S271K101

10 Boost Choke Layout

Core: CS468125 toriod Turns: 83

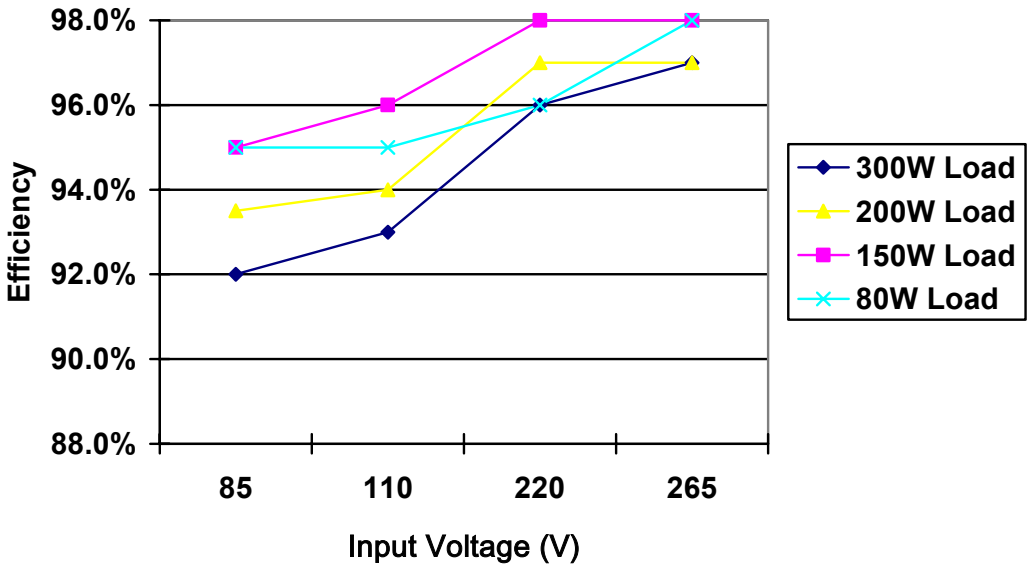
Wire: 1 x Φ1.0mm, AWG19 Inductance: L=1.24mH

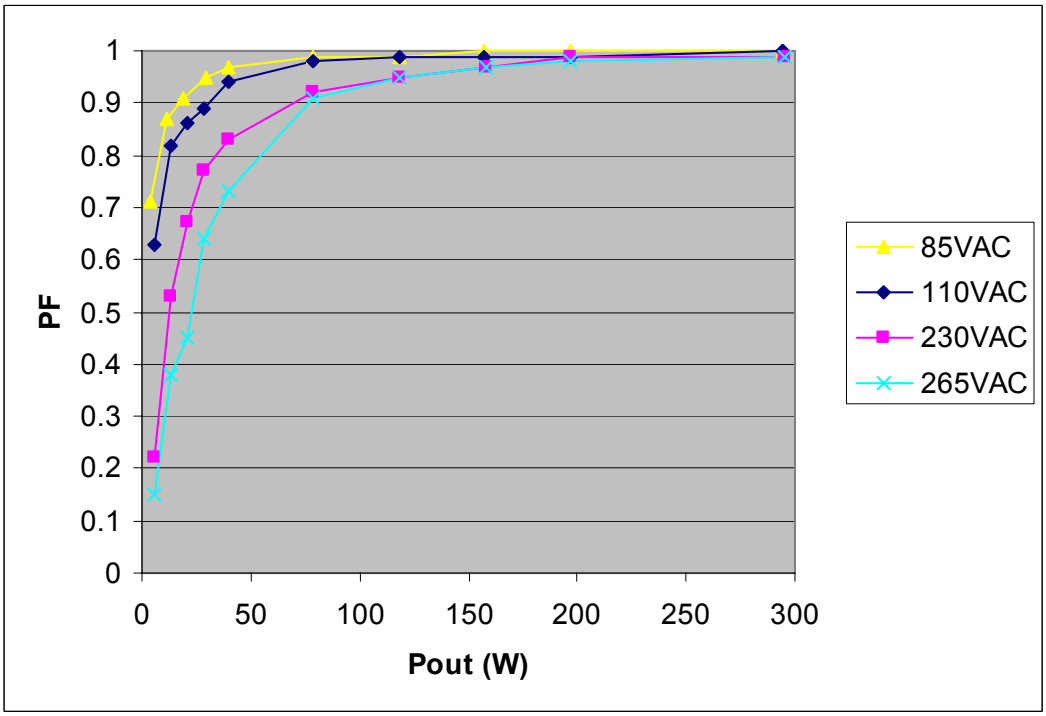
11 Test report

11.1 Load test (table and figure):

Vin (VAC)	Pin (W)	Iin (A)	Vout (V)	Iout (A)	Pout (W)	efficiency	PF
	320	3.8	393	0.75	294.75	92%	1
	211	2.51	393	0.5	196.5	93%	1
	165	1.96	393	0.4	157.2	95%	1
	124	1.47	393	0.3	117.9	95%	0.99
	83	0.99	393	0.2	78.6	95%	0.99
	43	0.52	394	0.1	39.4	92%	0.97
	31	0.39	394	0.075	29.55	95%	0.95
	20.3	0.26	395	0.049	19.355	95%	0.91
	12.2	0.17	396	0.029	11.484	94%	0.87
85	4.2	0.07	396	0.01	3.96	94%	0.71
	316	2.9	393	0.75	294.75	93%	1
	208	1.91	393	0.5	196.5	94%	0.99
	163	1.5	393	0.4	157.2	96%	0.99
	123	1.13	393	0.3	117.9	96%	0.99
	83	0.77	393	0.2	78.6	95%	0.98
	42.3	0.4	393	0.1	39.3	93%	0.94
	30	0.29	394	0.0718	28.2892	94%	0.89
	22	0.22	394	0.0525	20.685	94%	0.86
	14.2	0.15	394	0.034	13.396	94%	0.82
110	6.2	0.076	394	0.014	5.516	89%	0.63
	307	1.4	394	0.75	295.5	96%	0.99
	204	1	394	0.5	197	97%	0.99
	161	0.8	394	0.4	157.6	98%	0.97
	120	0.63	394	0.3	118.2	99%	0.95
	82	0.45	394	0.2	78.8	96%	0.92
	41	0.29	394	0.1	39.4	96%	0.83
	29.5	0.16	395	0.072	28.44	96%	0.77
	21.7	0.133	395	0.053	20.935	96%	0.67
	14	0.1	395	0.033	13.035	93%	0.53
220	6	0.093	395	0.014	5.53	92%	0.22
265	305	1.2	394	0.75	295.5	97%	0.99
	203	0.79	394	0.5	197	97%	0.98
	161	0.63	394	0.4	157.6	98%	0.97
	120	0.48	395	0.3	118.5	99%	0.95
	81	0.34	395	0.2	79	98%	0.91
	41	0.21	395	0.1	39.5	96%	0.73

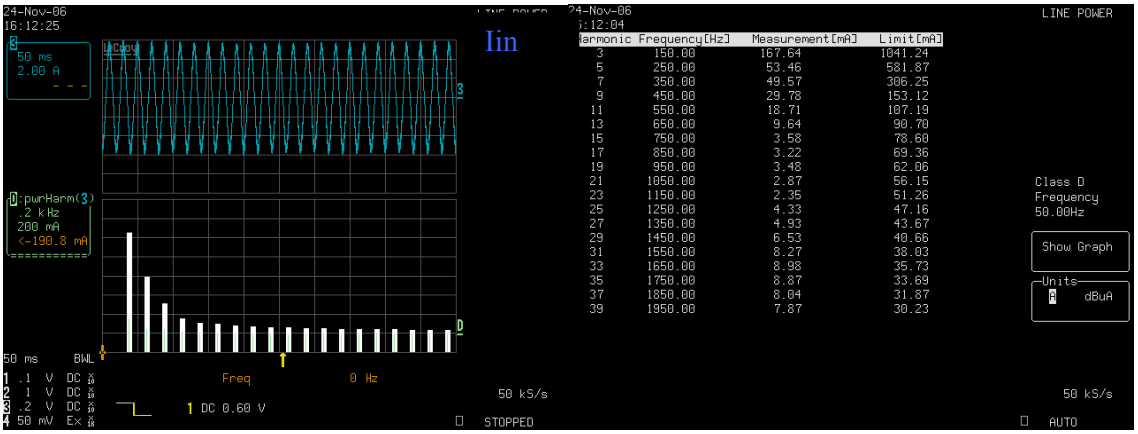
	29.5	0.17	395	0.072	28.44	96%	0.64
	21.7	0.16	395	0.053	20.935	96%	0.45
	13.8	0.15	395	0.033	13.035	94%	0.38
	5.83	0.1	395	0.014	5.53	95%	0.15





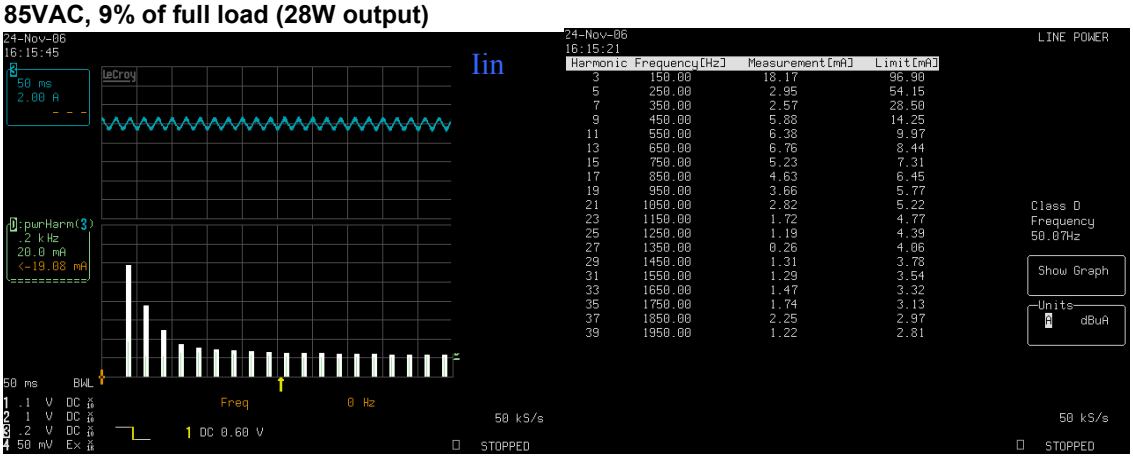
11.2 Harmonic test according to EN61000-3-2 Class D requirement

85VAC, full load (300W output)



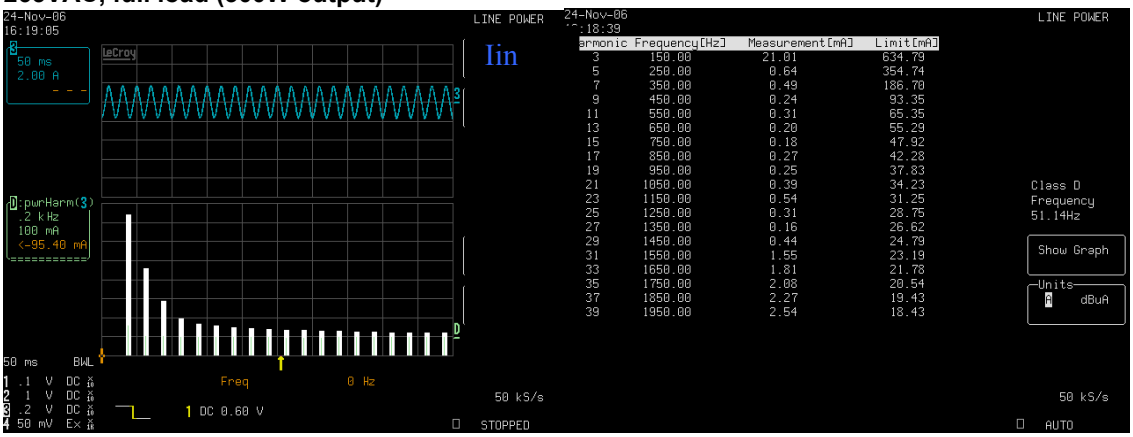
Harmonic	Frequency[Hz]	Measurement[mA]	Limit[mA]
3	150.00	167.64	1041.24
5	250.00	53.46	581.87
7	350.00	49.57	306.25
9	450.00	29.78	153.12
11	550.00	18.71	107.19
13	650.00	9.64	90.70
15	750.00	3.58	78.60
17	850.00	3.22	69.36
19	950.00	3.48	62.06
21	1050.00	2.87	56.15
23	1150.00	2.35	51.26
25	1250.00	4.33	47.16
27	1350.00	4.93	43.67
29	1450.00	6.53	40.66
31	1550.00	8.27	38.03
33	1650.00	8.98	35.73
35	1750.00	8.87	33.69
37	1850.00	8.04	31.87
39	1950.00	7.87	30.23

85VAC, 9% of full load (28W output)



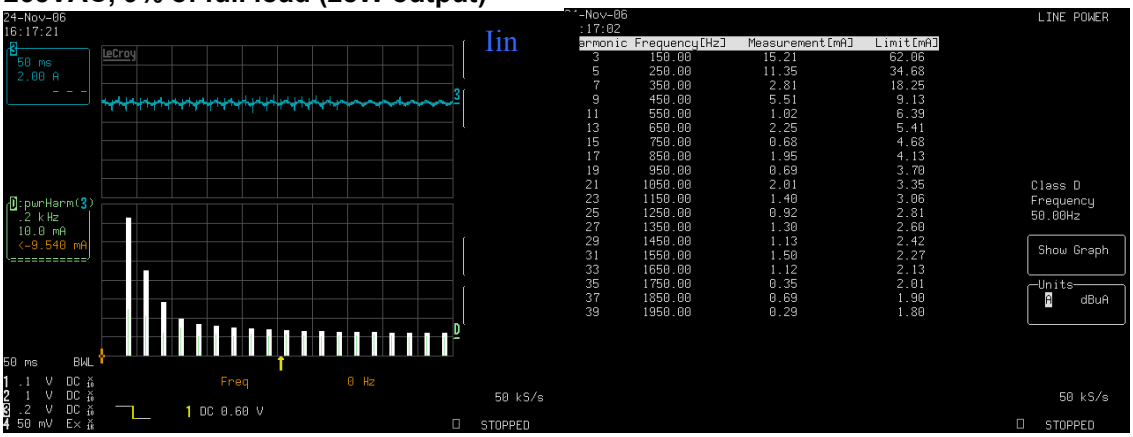
Harmonic	Frequency[Hz]	Measurement[mA]	Limit[mA]
3	150.00	18.17	96.90
5	250.00	2.95	54.15
7	350.00	2.57	28.50
9	450.00	5.88	14.25
11	550.00	6.38	9.97
13	650.00	6.76	8.44
15	750.00	5.23	7.31
17	850.00	4.63	6.45
19	950.00	3.66	5.77
21	1050.00	2.82	5.22
23	1150.00	1.72	4.77
25	1250.00	1.19	4.38
27	1350.00	0.26	4.06
29	1450.00	1.31	3.78
31	1550.00	1.29	3.54
33	1650.00	1.47	3.32
35	1750.00	1.74	3.13
37	1850.00	2.25	2.97
39	1950.00	1.22	2.81

265VAC, full load (300W output)



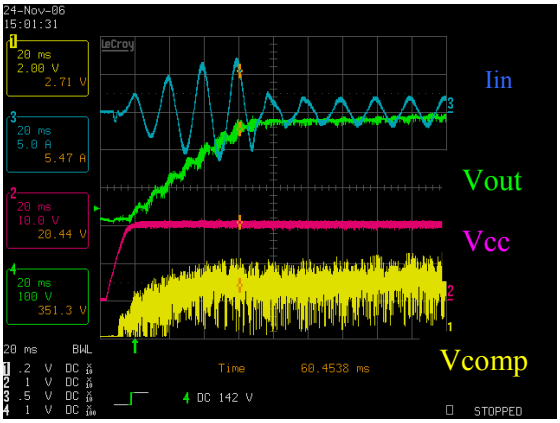
Harmonic	Frequency[Hz]	Measurement[mA]	Limit[mA]
3	150.00	21.01	634.79
5	250.00	0.64	354.74
7	350.00	0.49	186.70
9	450.00	0.24	93.35
11	550.00	0.31	65.35
13	650.00	0.20	55.29
15	750.00	0.18	47.92
17	850.00	0.27	42.28
19	950.00	0.25	37.83
21	1050.00	0.39	34.23
23	1150.00	0.54	31.25
25	1250.00	0.31	28.75
27	1350.00	0.16	26.62
29	1450.00	0.44	24.79
31	1550.00	1.55	23.19
33	1650.00	1.81	21.78
35	1750.00	2.08	20.54
37	1850.00	2.27	19.43
39	1950.00	2.54	18.43

265VAC, 9% of full load (28W output)

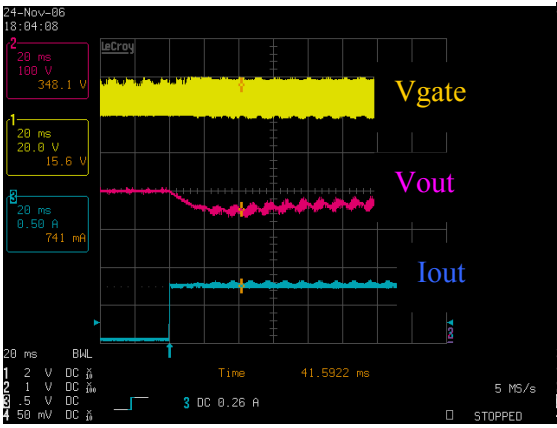


11.3 Waveforms (soft start, load jump, open loop)

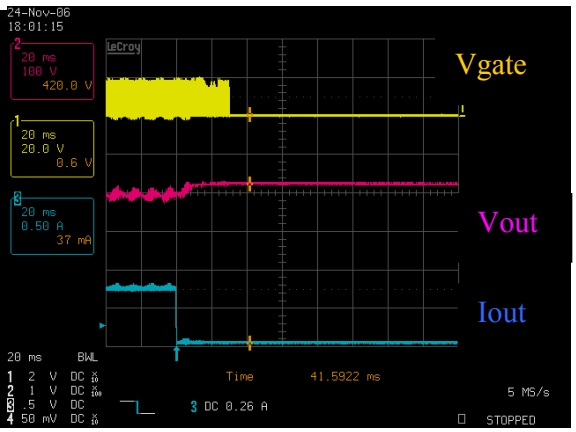
Soft start, test at 85VAC, Iout=0.2A



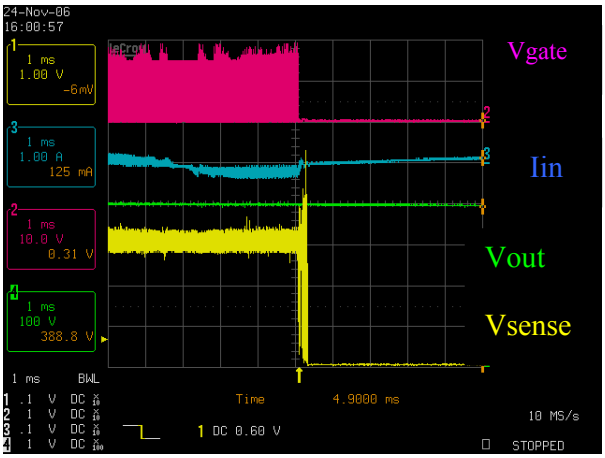
Load jump test at 85VAC, Iout from 0A to 0.75A



Load jump test at 85VAC, Iout from 0.75A to 0A



Open loop test at 265VAC, Iout=0.1A



12 References:

Design Guide for Boost Type CCM PFC with ICE2PCSxx

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Design Guide for Boost Type CCM PFC with ICE2PCSxx

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Luo Junyang
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Abstract

ICE2PCS01/02 are the 2nd generation of Continuous Conduction Mode (CCM) PFC controllers, which employ BiCMOS technology. Its control scheme does not need the direct sine-wave sensing reference signal from the AC mains compared to the conventional PFC solution. Average current control is implemented to achieve the unity power factor. In this application note, the design process for the boost PFC with ICE2PCXX is presented and the design details for a 300W output power PFC with the universal input voltage range of 85~265VAC are included.

1 Introduction

The Pin layout of ICE2PCS01 and ICE2PCS02 is shown in Figure 1.

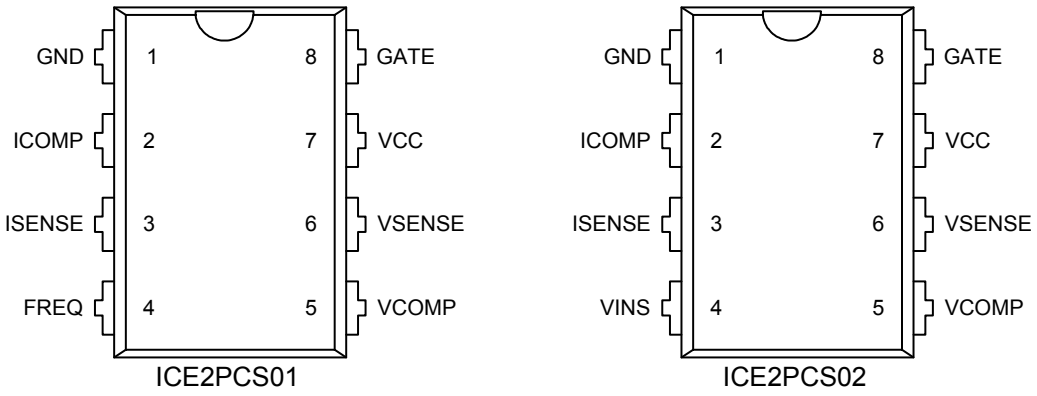


Figure 1 Pin Layout of ICE2PCS01 and ICE2PCS02

From the layout, it can be seen that most of Pins in ICE2PCS02 are the same as ICE2PCS01 except Pin 4. In ICE2PCS01, Pin 4 is to set the switching frequency. However, for ICE2PCS02, Pin 4 is for AC brown out detection and the switching frequency is fixed by internal oscillator at 65kHz. The typical application circuits of ICE2PCS01 and ICE2PCS02 are shown in Figure 2 and Figure 3 respectively.

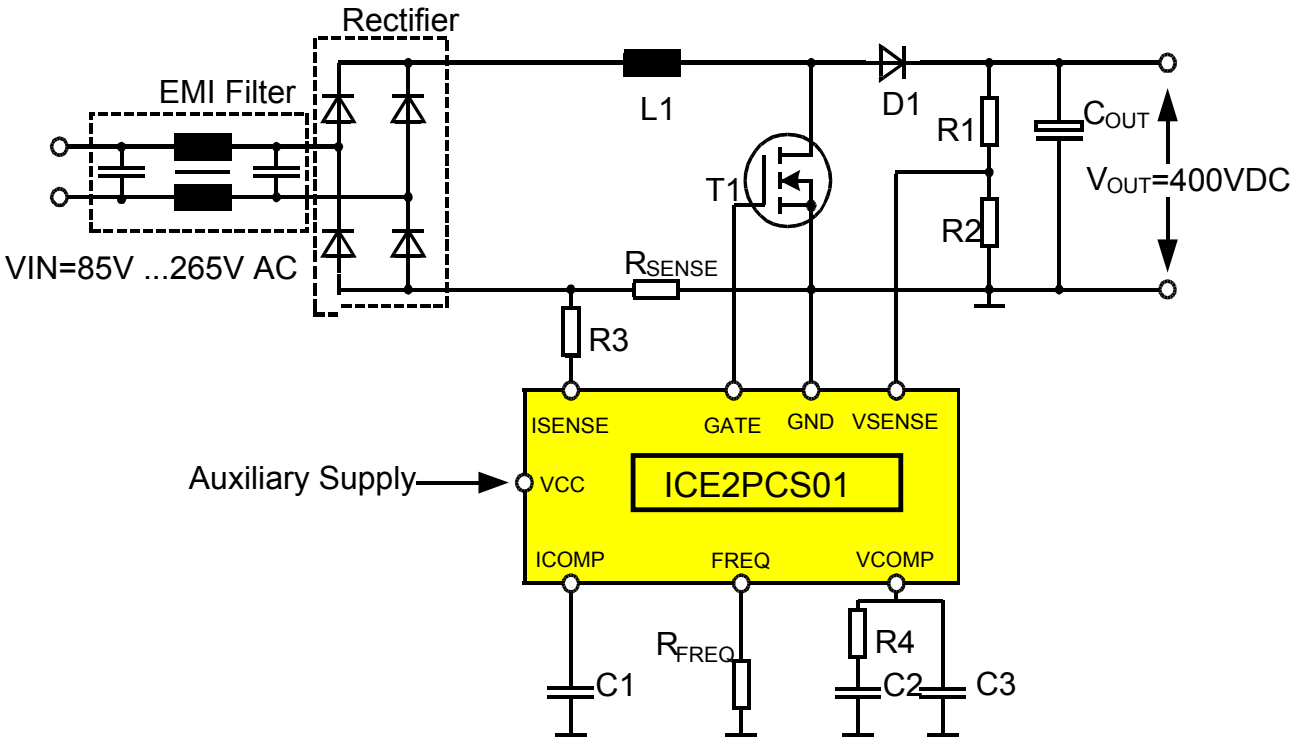


Figure 2 Typical application circuit of ICE2PCS01

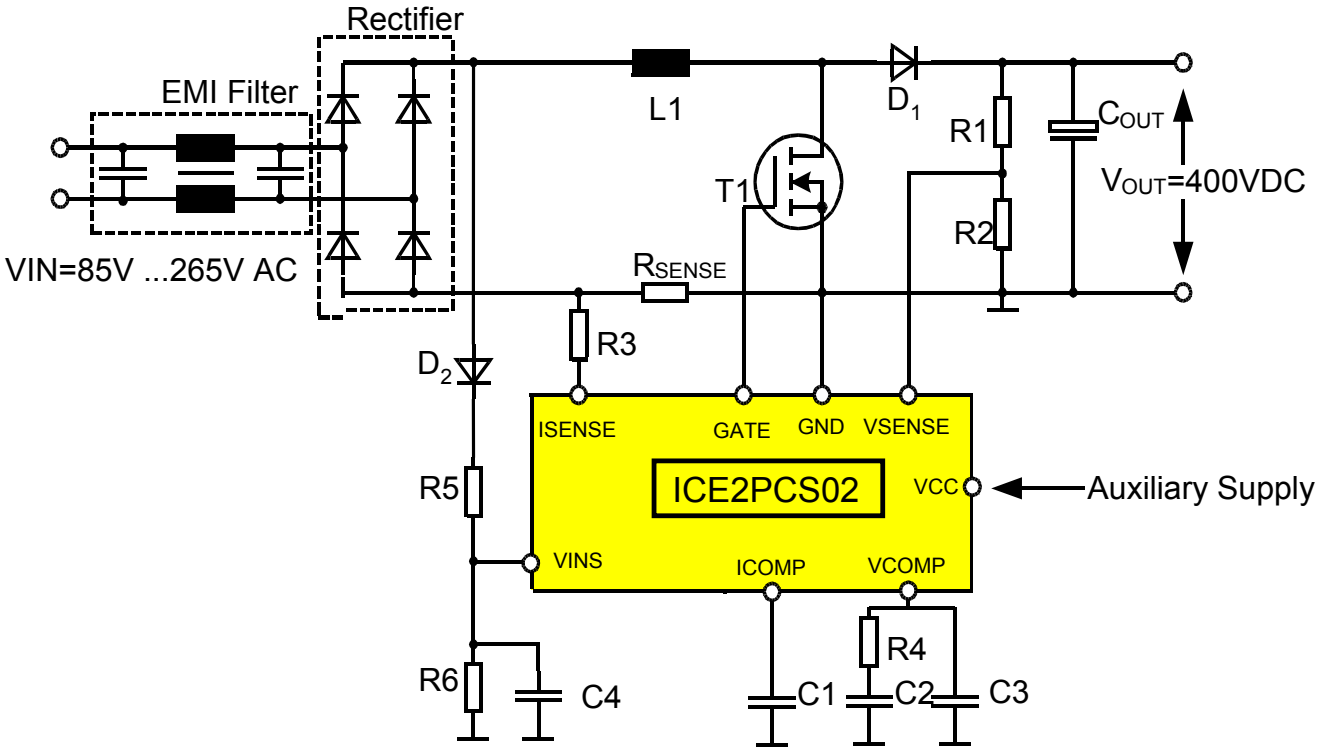


Figure 3 Typical application circuit of ICE2PCS02

2 Boost PFC design with ICE2PCXX

2.1 Target specification

The fundamental electrical data of the circuit are the input voltage range Vin, the output power Pout, the output voltage Vout, the operating switching frequency f_{SW} and the value of the high frequency ripple of the AC line current I_{ripple}. Table 1 shows the relevant values for the system calculated in this Application Note. The efficiency at rated output power Pout is estimated to 91 % over the complete input voltage range.

Input voltage	85VAC~265VAC
Input frequency	50Hz
Output voltage and current	390VDC, 0.76A
Output power	300W
Efficiency	>90% at full load
Switching Frequency	65kHz
Maximum Ambient temperature around PFC	70ºC

Table 1 Design parameter for the proposed design

2.2 Bridge rectifier

In order to obtain 300W output power at 85 V minimum AC input voltage, the maximum input RMS current is

$$I_{in\_RMS} = \frac{P_{out}}{V_{in\_min} \cdot \eta} = \frac{300}{85 \cdot 90\%} = 3.92A \quad (1)$$

and the sinusoidal peak value of AC current is

$$I_{in\_pk} = \sqrt{2} \cdot I_{in\_RMS} = \sqrt{2} \cdot 3.92 = 5.54A \quad (2)$$

For these values a bridge rectifier with an average current capability of 6A or higher is a good choice. Please note here, that due to a power dissipation of approximately

$$P_{BR} = 2 \cdot V_F \cdot I_{in\_RMS} = 2 \cdot 1V \cdot 3.92A = 7.84W \quad (3)$$

the rectifier bridge should be connected to an appropriate heatsink. Assuming a maximum junction temperature T_{Jmax} of 125°C, a maximum ambient temperature T_{Amax} of 70°C, the thermal junction-to-case R_{thJC} of approximate 2.5 K/W and the thermal case to heatsink R_{thCHS} of approximate 1K/W, the heatsink must have a maximum thermal resistance of

$$R_{thHS\_BR} = \frac{T_{J\max} - T_{A\max}}{P_{BR}} - R_{thJC} - R_{thCHS} = \frac{125 - 70}{7.84} - 2.5 - 1 = 3.52K/W \quad (4)$$

2.3 Power MOSFET and Gate Drive Circuit

Due to the switch mode operation, the loss is only valid during the on-time of the MOSFET. The duty cycle of the transistor in boost converters operating in CCM at minimum AC input RMS voltage is

$$D_{on} = 1 - \frac{V_{in\_min}}{V_{out}} = 1 - \frac{85}{390} = 0.782 \quad (5)$$

Since rms-values have the same effect on a system as DC-values, it is possible to calculate a characteristic duty cycle for the rms-value. Therefore, the on-state loss of the MOSFET in CCM-mode at a junction-temperature of 125°C is

$$P_{cond} = I_{in\_RMS}{}^2 \cdot D_{on} \cdot R_{dson(125C)} \quad (6)$$

the MOSFET switching loss can be estimated as

$$P_{SW} = (E_{on} + E_{off}) \cdot f_{SW} \quad (7)$$

where, E_{on} and E_{off} are the switch-on and switch-off energy loss which can be found in MOSFET datasheet, f_{SW} is the switching frequency.

For 300W design, if SPP20N60C3 is used, the conduction loss is

$$P_{cond} = 3.92^2 \cdot 0.782 \cdot 0.42 = 5.05W$$

assuming the switching current is about 6A and gate drive resistance Rg=3.6Ω, then the switching loss is

$$P_{SW} = (0.007mWs + 0.015mWs) * 65kHz = 1.43W$$

the total loss is

$$P_{MOS\_total} = P_{cond} + P_{SW} = 6.48W \quad (8)$$

the required heatsink for the MOSFET is

$$R_{thHS\_MOS} = \frac{T_{J\max} - T_{A\max}}{P_{MOS\_total}} - R_{thJC\_MOS} - R_{thCHS} = \frac{125-70}{6.48} - 0.6 - 1 = 6.89K/W \quad (9)$$

R_{thCHS} is the Rth of the insulation pad between MOSFET and heatsink.

Gate drive resistance is used to drive MOSFET as fast as possible but also keep dv/dt within EMI specification. In this 300W example, 3.6Ω gate resistor is chosen for SPP20N60C3 MOSFET.

Beside gate drive resistance, one 10kΩ resistor is also commonly connected between MOSFET gate and source to discharge gate capacitor.

2.4 Boost Diode

The boost diode D1 has big influence on the system's performance due to the reverse recovery behaviour. So the Ultra-fast diode with very low t_{rr} and Q_{rr} is necessary to reduce the switching loss. The new diode technology of silicon carbide (SiC) Schottky shows its outstanding performance with almost no reverse recovery behaviour. The switching loss due to the boost diode can be ignored with SiC Schottky diode. Only conduction loss is calculated as below.

$$P_{diode} = V_F \cdot I_{in\_RMS} \cdot (1 - D_{on}) = 2V \cdot 3.92A \cdot (1 - 0.782) = 1.71W \quad (10)$$

To decide the current rating of a SiC diode, there is a rule of thumb - the SiC diode can handle output power Pout of 100 W to120 W in a CCM-PFC-system per one rated ampere. For example, the SDT04S60 from Infineon Technologies is rated at a forward current IF = 4 A, so it is capable for a system of Pout = 4*100 W = 400 W system in minimum. Therefore, this diode should be suitable for the proposed design.

The required heatsink for boost diode is

$$R_{thHS\_diode} = \frac{T_{J\max} - T_{A\max}}{P_{diode}} - R_{thJC\_diode} - R_{thCHS} = \frac{125-70}{1.71} - 4.1 - 1 = 27.06K/W \quad (11)$$

The SiC boost diodes often have a poor surge current handling capability. Therefore a so called bypass diode is necessary such as the diode D3 as Figure 4. For the proposed system, 1N5408 is suitable.

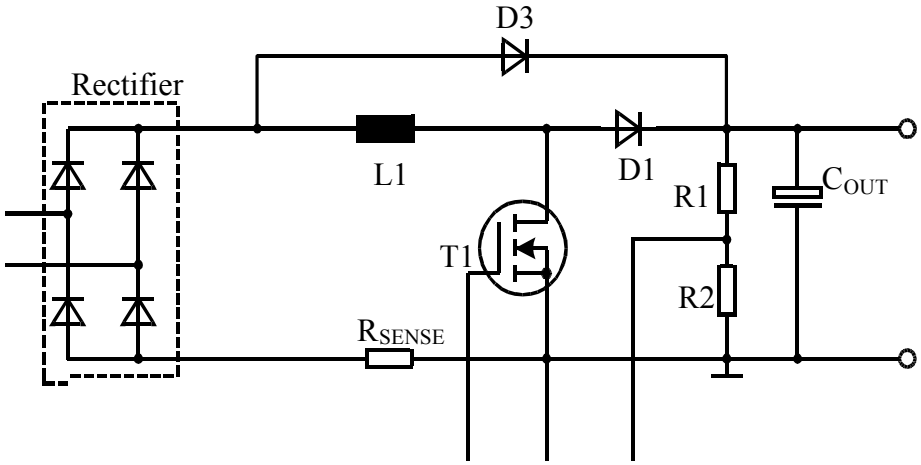


Figure 4 inrush current bypass diode

2.5 Boost inductor

The peak current that the inductor must carry is the peak line current at the lowest input voltage plus the high frequency ripple current. The high frequency ripple current peak to peak, I_{HF}, can be related to maximum input power and minmum input voltage as equation below.

$$I_{HF} = k \cdot \sqrt{2} \cdot \frac{P_{in\_\max}}{V_{in\_\min}} \tag{12}$$

Where, k must be kept reasonably small, and is usually optimized in the range of 15% to 25% for cost effective design based on the current magnetic component status. If k is too high, the larger AC input filter is required to filter out this ripple noise. If k is too low, the value of the inductance is too large and leads to big size of the magnetic core.

For example, we choose k = 22%, then,

$$I_{HF} = 22\% \cdot \sqrt{2} \cdot \frac{P_{in\_\max}}{V_{in\_\min}} = 1.2A$$

The peak current passing through inductor is

$$I_{L\_pk} = I_{in\_peak} + \frac{I_{HF}}{2} = 5.54 + \frac{1.2}{2} = 6.14A \tag{13}$$

The boost choke inductance must be

$$L_{boost} \geq \frac{D \cdot (1-D) \cdot V_{out}}{I_{HF} \cdot f_{SW}} \tag{14}$$

D=0.5 will generate the maximum value for the above equation.

$$L_{boost} \geq \frac{0.5 \cdot (1-0.5) \cdot 390V}{1.2A \cdot 65kHz} = 1.25mH$$

The magnetic core of the boost choke can be either magnetic powder or ferrite material.

(1) sendust powder toroid core

The required effective magnetic volume of the core, V_e, is

$$V_e \geq \mu_r \mu_0 L_{boost} (\frac{I_{L\_pk}}{B_{\max}})^2 = 125 \cdot 1.257e-6 \cdot 1.25mH (\frac{6.14A}{0.8T})^2 = 11.6e-6m^3 = 11.6cm^3 \quad (15)$$

where, μ_r is the relative permeability of the material. It should be noted that μ_r changes with different DC magnetizing force H, and so does the inductance. As an example, Figure 5 illustrates the relationship between the Percent Permeability and the DC Magnetizing Force H.

μ_0 in (15) is the magnetic field constant which is equal to 1.257e-6; B_{max} is the maximum magnetic flux density for the selected magnetic material (for sendust, B_{max} is up to 0.8T.)

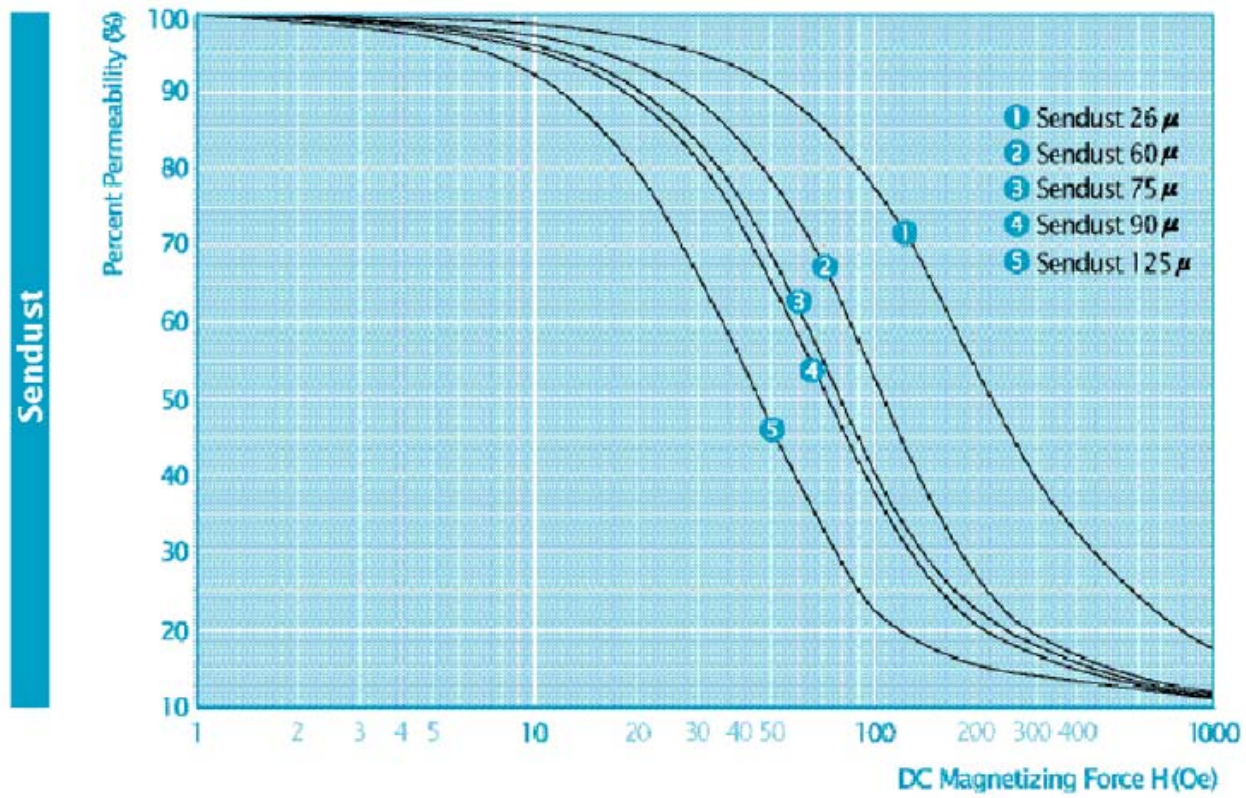


Figure 5 Percent Permeability and DC Magnetizing Force H (from Changsung)

Select a core with similar Ve value from the magnetic core datasheet. For example, the core type CS468125 from Chang Sung Corporation is selected. The parameters of CS468125 are V_e=15.584cm^3, A_e=1.34cm^2, C=11.63cm, μ_r=125. The turn number of the boost choke winding is

$$N_{toroid\_boost} = \sqrt{\frac{L_{boost} \cdot C}{\mu_r \mu_0 A_e}} = 83 \quad (16)$$

where, C is the magnetic path length and A_e is the effective magnetic cross section area.

To check the actual μ_r at low line, maximum power, the DC Magnetizing Force H is calculated

$$H = \frac{NI_{in\_pk}}{C} = 50(Oe)$$

Then μ_r = 125 * 50% = 62.5 according to Figure 5. The actual inductance can be re-calculated as $L_{boost} = \frac{N^2 \mu_r \mu_0 A_e}{C} = 0.625mH$. Hence, the corresponding ripple current will be higher than the previously assumed value.

The copper loss of the winding wire can be calculated on I_{in_RMS}.

$$P_{L\_boost} = I_{in\_RMS}^{\ 2} \cdot R_{L\_boost} \tag{17}$$

Select the proper wire type to fullfil the loss and thermal requirement for the choke.

(2) ferrite core

To make sure the ferrite core will not go into saturation, the turn number of the boost choke winding with ferrite core is

$$N_{ferrite\_boost} \geq \frac{I_{L\_pk} \cdot L_{boost}}{B_{\max} \cdot A_{\min}} \tag{18}$$

where, B_{max} is up to 0.3T according to ferrite material specification; A_{min} is the minimum magnetic cross section area.

The winding wire copper loss calculation is the same as in the above section of sendust powder toroid core.

2.6 AC line current filter

As decribed in section 2.5, there is high frequency ripple current peak to peak I_{HF} passing through boost choke. This ripple will also go into AC line power network. The current filter is necessary to reduce the amplitude of high frequency current component. The filtering circuit consists of a capacitor and an inductor as shown in Figure 6.

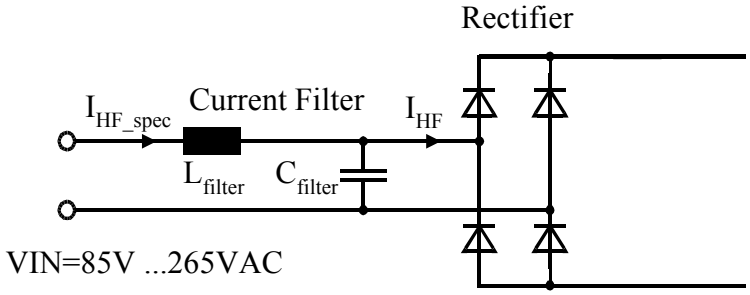


Figure 6 AC line current filter

The required L_{filter} is

$$L_{filter} \geq \frac{\frac{I_{HF}}{I_{HF\_spec}} + 1}{(2\pi f_{SW})^2 C_{filter}} \tag{19}$$

normally there is one EMI X2 capacitor which can act as C_{filter}. In this example, if we define I_{HF_spec} as 0.2A peak to peak and asumming X2 capacitance 0.47μF, then

$$L_{filter} \geq \frac{\frac{1.2A}{0.2A} + 1}{(2\pi \cdot 65kHz)^2 \cdot 0.47\mu F} = 89\mu H$$

The leakage inductance of EMI common mode choke can be used for current filter. If the leakage inductance is large enough, no need to add the additional differential mode inductor for filtering. Otherwise, a current filter choke is necessary. The calculation method for the current filter choke is the same as for boost choke.

2.7 Boost Output Bulk Capacitance

The bulk capacitance has to fullfil two requirements, output double line frequency ripple and holdup time.

(1) output double line frequency ripple limit.

The inherent PFC always presents 2*f_L ripple. The amplitude of ripple voltage is dependant on output current and bulk capacitance as below.

$$C_{out} \geq \frac{I_{out}}{\pi \cdot 2 * f_L \cdot V_{out\_ripple\_pp}} \tag{20}$$

where, I_{out} is the PFC output current, $V_{out\_ripple\_pp}$ is the output voltage ripple (peak to peak), and f_L is the AC line frequency.

Please note that ICE2PCXX has enhance dynamic block which is active when Vout exceed ±5% of regulated level. The enchanc dynamic block should be designed to work only during load or line change. During steady state with constant load, the enhance dynamic block should not be triggered, otherwise THD will be deteriorated. That means the target $V_{out\_ripple\_pp}$ must be lower than 10% of V_{out}. For this example, Vout=390VDC, then $V_{out\_ripple\_pp}$ must be lower than 39V. if we define $V_{out\_ripple\_pp}$=12V, then

$$C_{out} \geq \frac{I_{out}}{\pi \cdot 2 \cdot f_L \cdot V_{out\_ripple\_pp}} = 220\mu F \tag{21}$$

(2) holdup time requirement

After the PFC stage, there is commonly a PWM stage to provide isolated DC output for end user. Some applications, especially computing, have the holdup time requirement. It means that PWM stage should be able to provide the isolated output even if AC input voltage become zero for a short holdup time. The common specification for this holdup time is 20ms. If minimum input voltage for PWM stage is defined as 250VDC, then the bulk capacitance will be

$$C_{out} \geq \frac{2 \cdot P_{out} \cdot t_{holdup}}{V_{out}^{\ 2} - V_{out\_\min}^{\ 2}} = \frac{2 \cdot 300W \cdot 20ms}{390^2 - 250^2} = 134\mu F \tag{22}$$

the final C_{out} capacitance should be higher value calculated from the above two requirements.

2.8 Current Sense Resistor

The current sense resistance is calculated based on the IC soft over current control threshold and peak current carried by boost choke.

When the Isense signal reaches the soft over control threshold, IC will reduce the internal control voltage and accordingly the duty cycle is reduced in the following cycles. Finally the boost choke current is limited. According to IC datasheet, soft over current control threshold is -0.68V maximum. So the current sense resistor should be

$$R_{sense} \leq \frac{0.68V}{I_{L\_pk}} = \frac{0.68V}{6.14A} = 0.11\Omega \tag{23}$$

According to Figure 2 and Figure 3, the transistor current as well as the diode current flows through R_{sense}. That means, when AC is powered up, a large negative voltage drop at R_{sense} will be observed when large inrush current in the range of about 150 A to 200 A flows through the resistor. It is therefore necessary to limit the current into Pin 2 (ISENSE) to 1 mA, which is realized with resistor R3. A value of R3 = 220Ω is sufficient for this resistor.

2.9 Output voltage sensing divider

The output voltage is set with the voltage divider represented by R_1 and R_2 in Figure 2 and Figure 3. First, choose the value of the lower resistor R_2. Then the value of the upper resistor R_1 is

$$R_1 = \frac{V_{out} - V_{ref}}{V_{ref}} \cdot R_2 \tag{24}$$

where, Vref is IC internal reference voltage for voltage sensing, 3V typical.

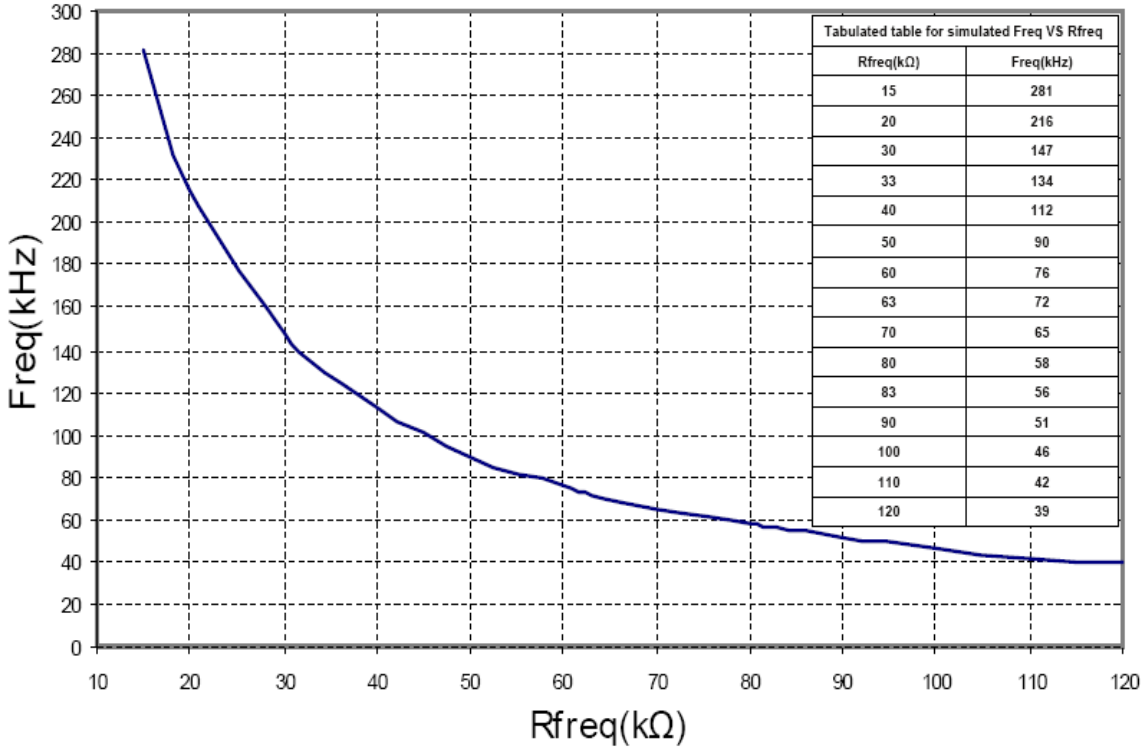
If R_2=6kΩ,

$$R_1 = \frac{390 - 3}{3} \cdot 10k\Omega = 774k\Omega$$

It is recommended to take resistor values with a tolerance of 1% for R_1 and R_2. Due to the voltage stress of R1, it is recommended to split this value into few resistors in series.

2.10 Frequency setting (only for ICE2PCS01)

The frequency of the ICE2PCS01 is adjustable in the range of 50 kHz up to 250 kHz. The external resistor R_{FREQ} according to Figure 7 programs a current which controls the oscillator.



Tabulated table for simulated Freq VS Rfreq

Rfreq(kΩ)	Freq(kHz)
15	281
20	216
30	147
33	134
40	112
50	90
60	76
63	72
70	65
80	58
83	56
90	51
100	46
110	42
120	39

Figure 7 Resistor-frequency characteristic

2.11 AC Brown-out Shutdown (only for ICE2PCS02)

Brown-out occurs when the input voltage VAC falls below the minimum input voltage of the design (i.e. 85V for universal input voltage range) and the VCC has not entered into the VCCUVLO level yet. For a system without input brown out protection (IBOP), the boost converter will increasingly draw a higher current from the mains at a given output power which may exceed the maximum design values of the input current and lead to over heat of MOSFET and boost diode. ICE2PCS02 provides a new IBOP feature whereby it senses directly the input voltage for Input Brown-Out condition via an external resistor/capacitor/diode network as shown in Figure 8. This network provides a filtered value of VIN which turns the IC on when the voltage at Pin 4 (VINS) is more than 1.5V. The IC enters into the standby mode and gate is off when VINS goes below 0.7V. The hysteresis prevents the system to oscillate between normal and standby mode.

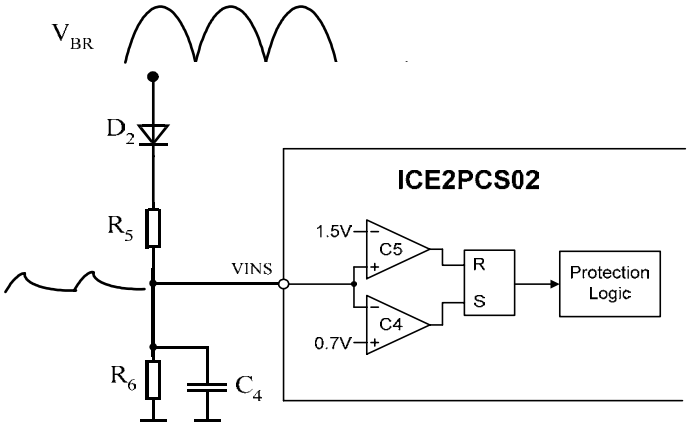


Figure 8 Block diagram of voltage loop

Because of the high input impedence of comparator of C4 and C5, R5 can be high ohmic resistance to reduce the loss. From the datasheet, the bias current on VINS Pin is 1μA maximum. In order to have the design consistence, the current passing through R5 and R6 has to be much higher than this bias current, for example 6μA. Then R6 is:

$$R_6 = \frac{0.7V}{6uA} = 117k\Omega \tag{25}$$

R6 is selected 120KΩ. R5 is selcted by

$$R_5 = \frac{\sqrt{2} \cdot V_{AC\_on} - 1.5V}{1.5V} \cdot R_6 \tag{26}$$

where, V_{AC_on} is the minimum AC input voltage (RMS) to start PFC, for example 70VAC.

$$R_5 = \frac{\sqrt{2} \cdot 70V - 1.5V}{1.5V} \cdot 120k\Omega = 7.8M\Omega$$

Due to the voltage stress of R_5, it is recommended to split this value into few resistors in series.

C_4 is used to modulate the ripple at the VINS pin. The timing diagram of VINS pin when IC enters brown-out shutdown is shown in Figure 9.

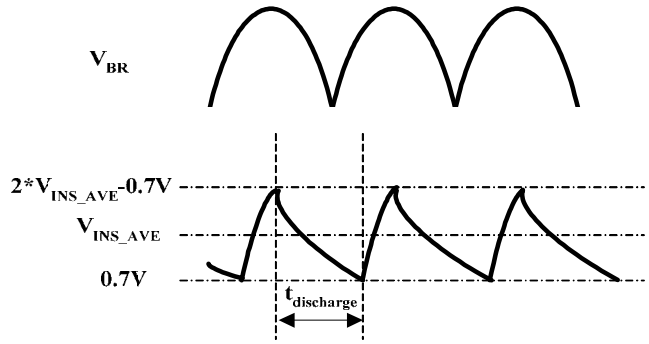


Figure 9 Timing diagram of VINS Pin when IC enters brown-out shutdown

If the bottom level of the ripple voltage touches 0.7V, PFC is in standby mode and gate is off. The ripple voltage defines PFC brown out off threshold of AC input voltage (RMS), V_{AC_off}. C_4 can be obtained from the following equation. Assuming $V_{INS\_AVE} = \frac{R_6}{R_5 + R_6} \cdot V_{AC\_off}$, where, V_{AC_off} is the maximum AC input voltage (RMS) to switch off PFC, for example 65VAC.

$$(2 \cdot \frac{R_6}{R_5 + R_6} \cdot V_{AC\_off} - 0.7) \cdot e^{-\frac{t_{discharge}}{R_6 C_4}} = 0.7V \tag{27}$$

assuming $t_{discharge}$ is equal to half cycle time of line frequency, ie. $t_{discharge} = \frac{1}{2 f_L}$, then

$$C_4 = \left(2 f_L R_6 \ln \frac{2 \cdot \frac{R_6}{R_5 + R_6} V_{AC\_off} - 0.7V}{0.7V} \right)^{-1}$$

$$C_4 = \left(2 \cdot 50Hz \cdot 120k\Omega \ln \frac{2 \cdot \frac{120k\Omega}{7.8M\Omega + 120k\Omega} 65V - 0.7V}{0.7V} \right)^{-1} = 140nF \tag{28}$$

2.12 IC supply

The IC supply voltage operating range is 11~26V.

There are two stages during IC turned on. First Vcc capacitor is charged from 0V to 7V, the IC internal regulator block starts to reset voltage at all external pins. The reset process will take about 10us. And then when Vcc voltage is charged to Vcc_on threshold, IC starts the soft start with gate switching. In the case of Vcc decoupling capacitance is too low such as 0.1uF, Vcc voltage may be charged up too fast and the time interval from Vcc=7V to Vcc_on is less than the reset time. Then the IC will not go through a proper soft start as the voltages at IC pins are not yet properly reset. To avoid such a problem, the delay circuitry is needed.

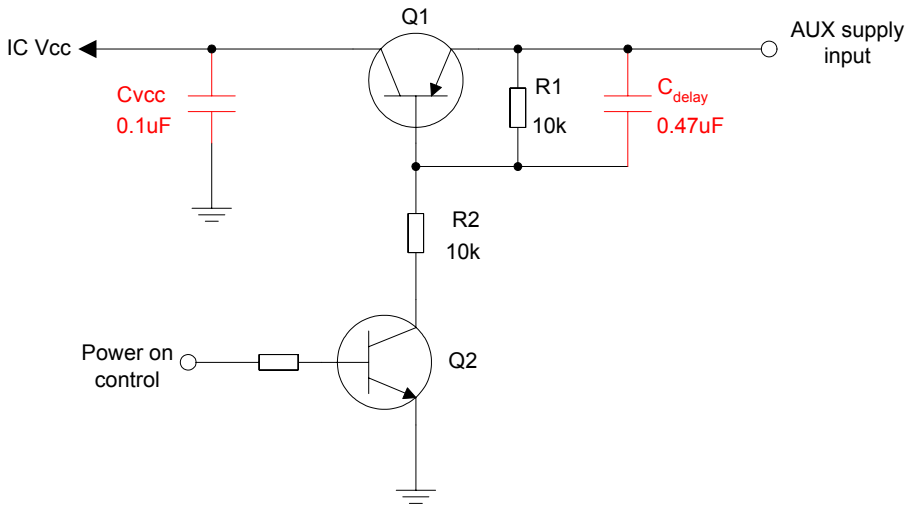


Figure 10 Vcc supply circuitry

Figure 10 is a typical circuitry to supply PFC controller. Q2 is NPN transistor and controlled by external "Power on" signal. When "Power on" signal is "high", Q2 is turned on provides base current for Q1. Q1 is turned on accordingly to supply auxiliary power to IC Vcc. The reset delay time is adjustable by changing the RC time constant of R1, R2 and C_{delay}. The recommended values are shown in Figure 10 as 10kΩ, 10kΩ and 0.47uF respectively.

The same reset process also happens during IC power down when Vcc is discharged from Vcc_off to 7V. The reset time for power down is around 200us. Because IC is in power down mode with very low current consumption, typically 300uA only, the required Vcc capacitance for power down reset can be calculated as:

$$C_{VCC} \geq \frac{I_{power\_down\_max} \cdot t_{reset}}{V_{cc\_off\_min} - V_{reset}} = \frac{650\mu A \cdot 200\mu s}{10.4V - 7V} = 38.2nF \quad (29)$$

So the common Vcc decoupling capacitance 0.1uF is enough for reset delay requirement.

2.13 PCB layout guide

In order to avoid crosstalk on the board between power and signal path, and to keep the IC GND pin as "clean" from noise as possible, the PCB layout for GND must be taken care of properly. Below are some suggestions for GND connection and Figure 11 below illustrates as a good example.

(1) Star connection rule for main power stage GND: the PCB tracks of MOSFET source, output load GND, IC auxiliary supply GND and shunt resistor are separated and connected together at bulk capacitor negative Pin.

(2) Star connection rule for small signal IC GND: the IC external components which need to be connected to the small signal GND bus highlighted in red color. Such GND bus is connected to IC GND Pin.

(3) Connection between main power stage GND and small signal IC GND: in Figure 11, a single PCB track in pink color directly connect IC GND pin to power stage star connection point - bulk capacitor negative. This is to ensure that the voltage between IC Isense Pin and IC GND Pin does not observe the switching rectangular noise current. The dark green and blue tracks denote for flowing paths of high frequency rectangular switching current.

(4) Vcc decoupling capacitor Cvcc: the decoupling capacitor need to be placed close to IC Vcc and GND Pins as much as possible. The GND track of Cvcc (green color in Figure 11) should be connected at the point on the single PCB track connecting between IC GND Pin and power GND point so that the large gate charging current will not pass through the small signal GND bus.

(5) Vsense capacitor Cvsense: to reduce noise in Vsense Pin, small capacitor up to 0.1uF can be added between Vsense Pin and small signal GND bus.

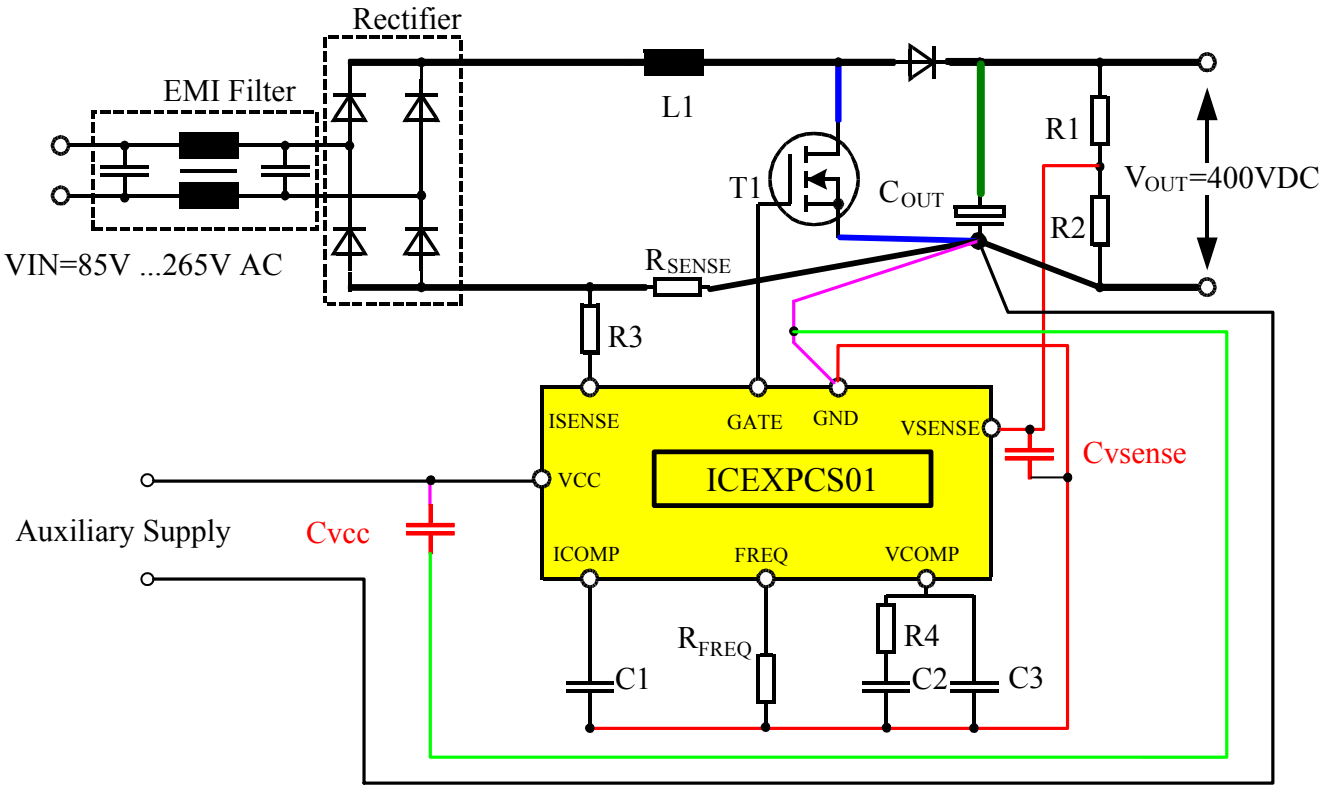
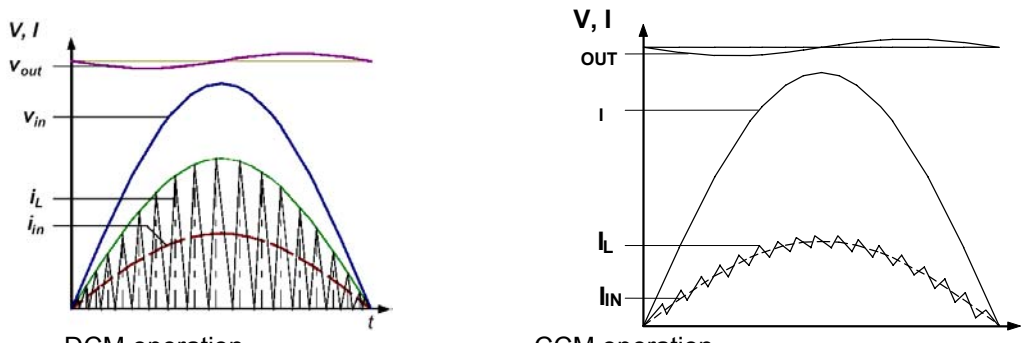


Figure 11 Good PCB layout illustration

3 Voltage loop and current loop compensation

This section provides a model and a tool for evaluating and improving the control loop characteristics of ICE2PCS02-based PFC pre-regulators in boost topology. The goal is not only to ensure a narrow bandwidth in order to achieve a high Power Factor, but also to have enough phase margin so as to make sure the system is stable over a large range of operating conditions. The design example is demonstrated as well.

Traditional diode rectifiers used in front of the electronic equipment draw pulsed current from the utility line, which deteriorates the line voltage, produce radiated and conducted electromagnetic interference, leads to poor utilization of the capacity of the power sources. In compliance with IEC 61000-3-2 harmonic regulation, active power factor correction (PFC) circuit is getting more and more attention in recent years. For low power up to 200W, discontinuous conduction mode (DCM) PFC is popular due to its lower cost. Furthermore, there is only one control loop, i.e. voltage loop, in its transferring control blocks. The design is easy and simple for DCM operation. However, due to its inherent high current ripple, DCM is seldom to be used for high power applications. In high power applications, continuous conduction mode (CCM) PFC is more attractive.



DCM operation CCM operation

Figure 12 DCM and CCM PFC principle

3.1 How to achieve PFC function without sinusoidal reference sensing

3.1.1 Boost converter modeling

Figure 13 shows the inductor current waveform for boost converter operating in continuous conduction mode.

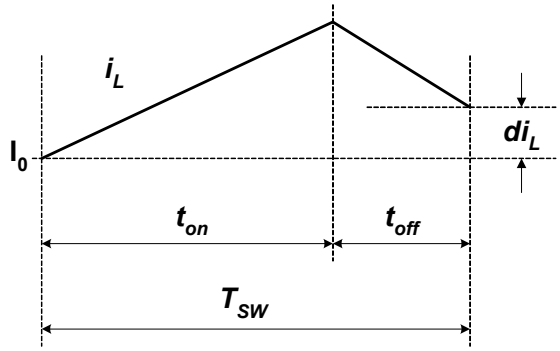


Figure 13 inductor current waveform of boost converter operating in CCM mode

assuming Vin is boost converter input DC voltage, Vout is the boost converter output voltage, L is the boost choke inductance, ton is the on time duration in one switching cycle, toff is the off time duration in one switching cycle, doff is the off time duty cycle and Tsw is the time duration in one switching cycle.

During “on” interval,

$$\frac{di_L}{dt} = \frac{V_{in}}{L} \tag{30}$$

During “off” interval,

$$\frac{di_L}{dt} = \frac{V_{in} - V_{out}}{L} \tag{31}$$

And then the boost inductor current variation after one switching cycle is:

$$di_L = \frac{V_{in}}{L} \cdot t_{on} + \frac{V_{in} - V_{out}}{L} \cdot t_{off} = \frac{V_{in} - V_{out} \cdot d_{off}}{L} \cdot T_{SW} \tag{32}$$

The instant boost inductor current after n switching cycle is:

$$i_{L\_n} = i_{L\_n-1} + \frac{V_{in\_n} - V_{out\_n} \cdot d_{off\_n}}{L} \cdot T_{SW} \tag{33}$$

3.1.2 PFC IC control principle with boost topology

PFC IC control block is inserted in boost converter as shown in Figure 14.

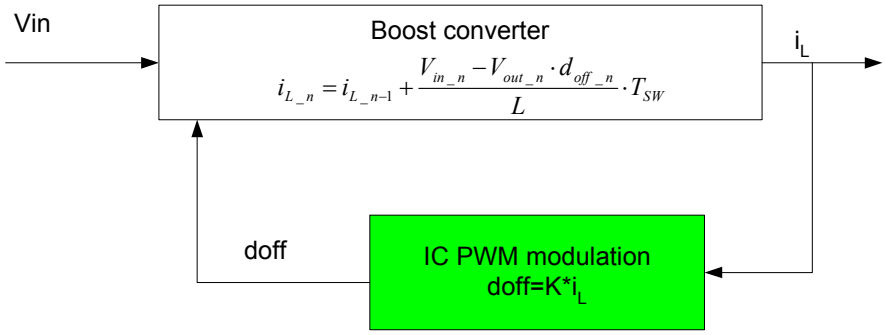


Figure 14 PFC current loop principle

IC senses boost inductor average current, and calculate the off duty cycle to be proportional to inductor current, and then send such off duty cycle back to boost converter. The negative feedback loop can be seen from Figure 14. A small disturb increasing on i_L will result in a little bit increasing on off duty cycle. The increasing off duty cycle will lead to decreasing of i_L after processing by boost converter. In the stead state,

$$V_{in} = V_{out} \cdot d_{off} = V_{out} \cdot K \cdot i_L \quad (34)$$

Where, K is the modulation gain defined by IC. It can be seen that boost inductor current shape follows AC input voltage and it is how PFC function to be achieved.

In the following sections, detail mathematical analysis of current loop and voltage loop will be described and the transfer function for each block is given in order to design IC external compensation network components.

3.2 Current Loop Regulation and Transfer Function

The detail block diagram of current loop for ICE2PCS02 is shown in the Figure 15. The boost converter stage K_{boost} is elaborated in S-plane.

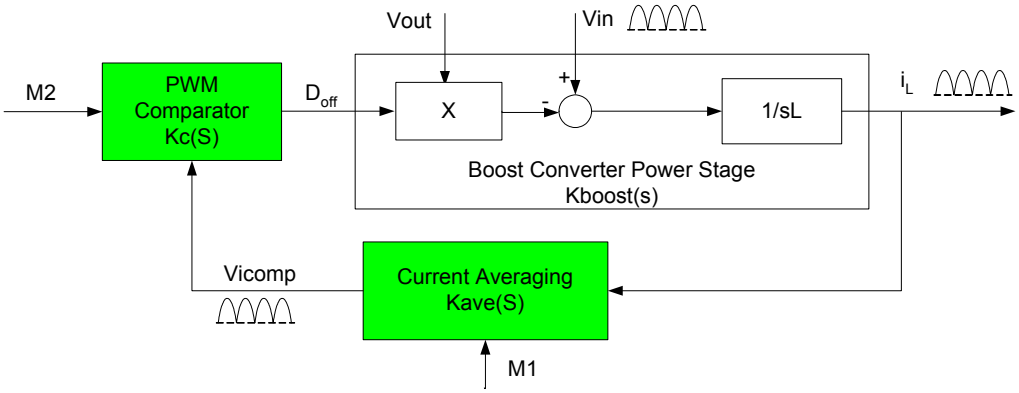


Figure 15 Block diagram of current loop

3.2.1 Current Averaging Circuit

IC sense the boost inductor current via shunt resistor Rsense as shown in Figure 2. The sensing signal is sent to Isense Pin. As the voltage in Isense Pin is negative signal together with switching ripple, IC need to do signal averaging and convert the polarity to positive for following PWM modulation blocks. The output of averaging block is Vicomp voltage at Icomp Pin. the block diagram of current averaging block is shown in Figure 16.

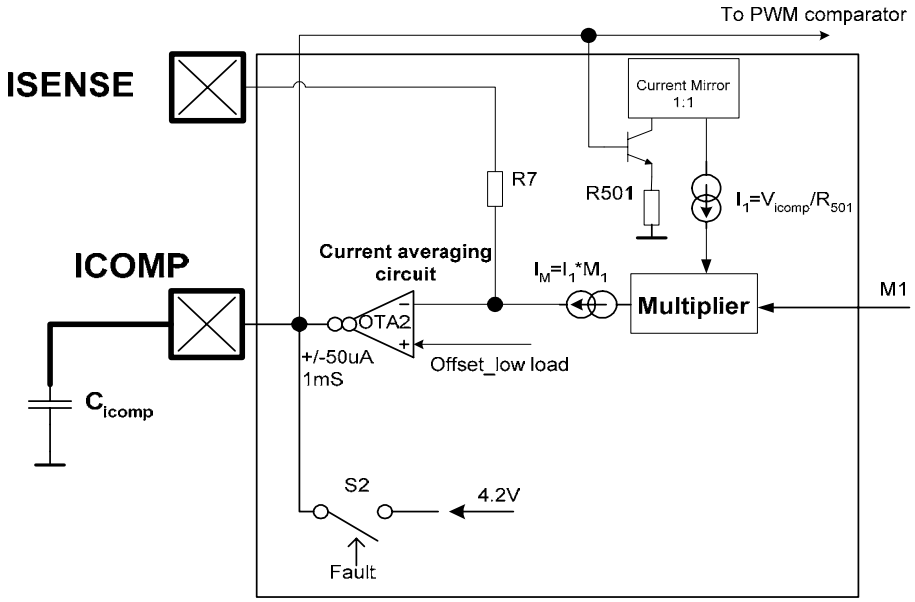


Figure 16 current averaging block diagram

The transfer function of averaging circuit block can be derived as below.

$$K_{AVE}(s) = \frac{V_{icomp}}{i_L} = \frac{\frac{K_1 R_{sense}}{M_1}}{1 + s \cdot \frac{K_1 C_{icomp}}{M_1 g_{OTA2}}} \tag{35}$$

where, K_1 is a ratio between R501 and R7 which is equal to 4, C_{icomp} is the capacitor at Icomp Pin, g_{OTA2} is the trans-conductance of the error amplifier of OTA2 for current averaging, typical 1.0mS as shown in Datasheet, M1 is the variable controlled by voltage loop.

The function of the averaging circuit is to filter out the switching current ripple. So the corner frequency of the averaging circuit f_{AVE} must be lower than the switching frequency f_{SW}. Then,

$$C_{icomp} \geq \frac{g_{OTA2} M_1}{K_1 \cdot 2\pi f_{AVE}} \tag{36}$$

3.2.2 PWM comparator block

The averaged Vicomp signal is sent to PWM comparator block and compared with internal triangular ramp signal to derive duty cycle. The timing diagram of this block is shown in Figure 17.

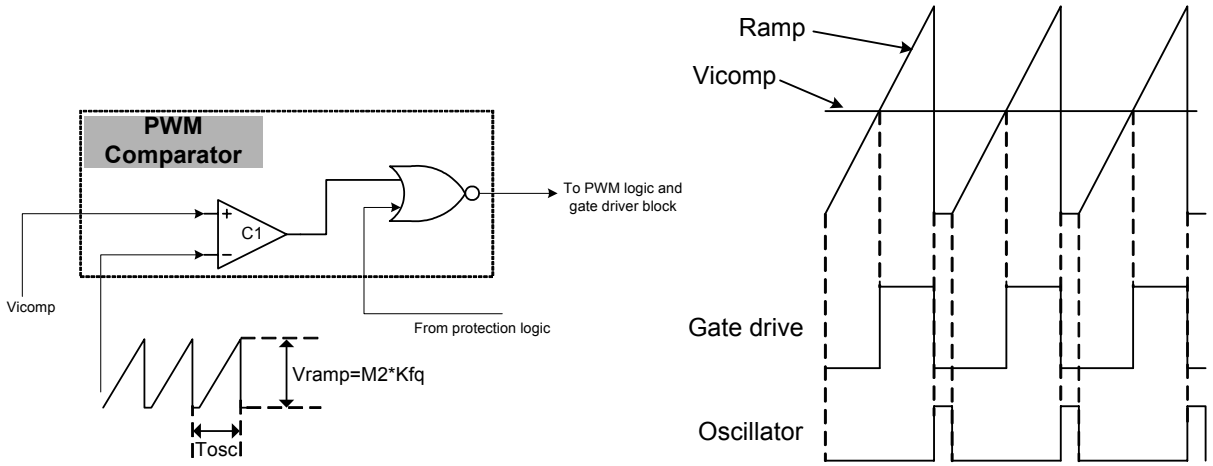


Figure 17 The block diagram and timing sequence of PWM comparator block

The operating principle is explained as following. Gate output is in “low” state in the beginning of the each cycle. Gate output is turned to “high” at the intersection of the triangular ramp signal and Vicomp signal. Gate output is turned to “low” by oscillator synchronous signal. Based on the operating principle, the transfer function of $K_C(s)$ is:

$$K_C(s) = \frac{d_{off}}{V_{icomp}} = \frac{1}{K_{FQ} M_2} \tag{37}$$

Where, K_{FQ} is a design constant which is equal to 9.183, M_2 is the variable controlled by voltage loop.

3.2.3 Boost converter stage

The transfer function of boost converter stage $K_{Boost}(s)$ can be obtain via State-Space Averaging method. Combining equation (30) and (31) by state –space averaging,

$$\frac{di_L}{dt} = \frac{V_{in}}{L} d_{on} + \frac{V_{in} - V_{out}}{L} d_{off} = \frac{V_{in} - V_{out} d_{off}}{L} \tag{38}$$

Make Laplace transformation for equation (38) with assuming Vin and Vout are constant for current loop analysis,

$$i_L(s) = (V_{in} - V_{out} d_{off}(s)) \frac{1}{sL} \tag{39}$$

The equation (39) has been described in current loop block diagram in Figure 15. **Although Vin is not physically sensed by circuit, the input sinusoidal signal is presented in transfer functions only if boost topology is applied.**

3.2.4 Open loop transfer function gain for current loop

The open loop gain of current regulation loop is:

$$G_C(s) = K_{AVE}(s) K_C(s) \frac{V_{out}}{sL} = \frac{\frac{K_1 R_{sense} V_{out}}{K_{FQ} M_1 M_2 L}}{s(1 + s \cdot \frac{K_1 C_{icomp}}{M_1 g_{OTA2}})} \tag{40}$$

The selected C_{icomp} must also meet the requirement that the cross over frequency of the current loop f_C is much lower than the switching frequency f_{SW}.

3.2.5 Steady state solution of I_L

Solving the current loop in Figure 15,

$$i_L(s) = (V_{in} - V_{out} d_{off}(s)) \frac{1}{sL} = (V_{in} - V_{out} K_C(s) K_{AVE}(s) i_L(s)) \frac{1}{sL}$$

$$i_L(s) = \frac{\frac{V_{in}}{sL}}{1 + \frac{V_{out} K_C(s) K_{AVE}(s)}{sL}} = \frac{\frac{V_{in}}{sL}}{1 + G_C(s)} \tag{41}$$

For AC line frequency which is much lower than f_C, then $|G_c(s)| >> 1$

$$i_L(s) = \frac{\frac{V_{in}}{sL}}{1 + G_C(s)} \approx \frac{\frac{V_{in}}{sL}}{G_C(s)} = \frac{\frac{K_{FQ} M_1 M_2 V_{in}}{K_1 R_{sense} V_{out}}}{1 + s \cdot \frac{K_1 C_{icomp}}{M_1 g_{OTA2}}} \tag{42}$$

For AC line frequency which is also much lower than f_{AVE}, $\left| s \cdot \frac{K_1 C_{icomp}}{M_1 g_{OTA2}} \right| << 1$, then the steady state I_L can be derived as

$$I_L = \frac{K_{FQ} M_1 M_2 V_{in}}{K_1 R_{sense} V_{out}} \tag{43}$$

from the above steady state solution of I_L, it can be seen that the choke current I_L is always following input voltage V_{in}. This is how PFC function is achieved.

3.3 Voltage Loop Compensation

The control loop block diagram for ICE2PCS02 based CCM PFC is shown in Figure 18 and Figure 19. There are four blocks in the loop. IC PWM Modulator $G_2(s)$ has been discussed in above Section 3. the rest of them are Error Amplifier $G_1(s)$, nonlinear block $G_{NON}(s)$, boost converter output stage $G_3(s)$ and Feedback Sensing $G_4(s)$.

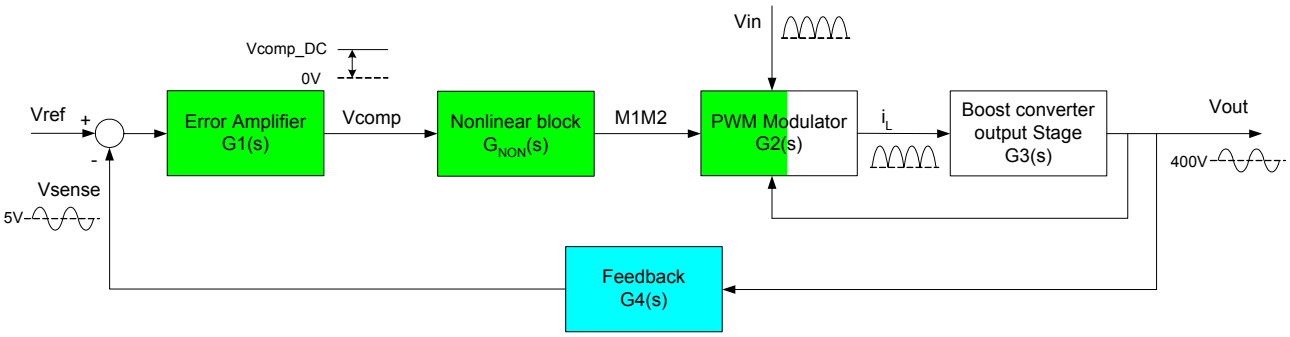


Figure 18 Large signal modeling of voltage loop

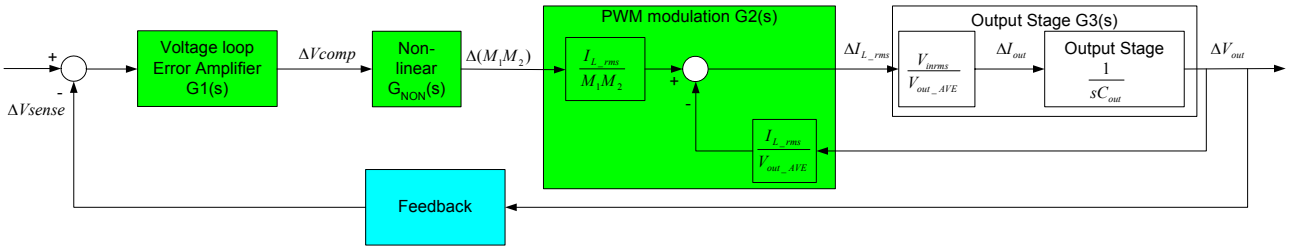


Figure 19 Small signal modeling of voltage loop

3.3.1 Boost converter output stage $G_3(s)$

Boost converter output stage is described as influencing of variation on i_L to bulk output voltage Vout. The transfer function of power stage, $G_3(s)$, is separated to two stages as:

$$G_3(s) = \frac{\Delta V_{out}}{\Delta I_{L\_rms}} = \frac{\Delta V_{out}}{\Delta I_{out}} \cdot \frac{\Delta I_{out}}{\Delta I_{L\_rms}} \tag{44}$$

where V_{out} is the DC output voltage, I_{out} the DC output current and I_{L_rms} is the boost inductor current.

3.3.1.1 ΔV_{out} / ΔI_{out}

Under the above assumption, the power stage can be modeled as illustrated in Figure 20: a controlled current source (with a shunt resistor Re) that drives the output bulk capacitor C_{out} and the load resistance Rout (= Vout / Iout). The zero due to the ESR associated with C_{out} is far beyond the crossover frequency thus it is neglected.

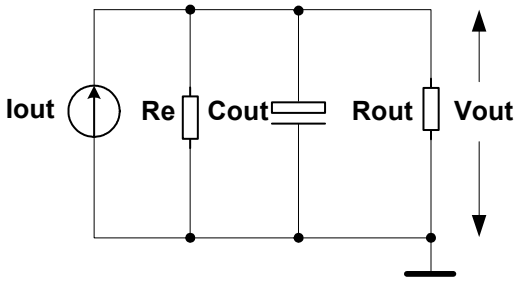


Figure 20 Power stage modeling

A few algebraic manipulations would show that the shunt resistor Re always equals the DC load resistance Rout, thus it changes depending on the power delivered by the system. There are two kinds of load in the application. Two cases will give a different result in case of resistive load or constant power load. For purely resistive load, the AC load resistance equals Ro. In case of constant power load like additional isolated PWM DC/DC converter, the AC load resistance is equal to -Ro (if the DC bus decreases, the current demanded of the PFC increases. hence the negative sign is shown.). As a result, the parallel combination with Re tends to infinity and the two resistances cancel. The current source drives only the output capacitor. The result is summarized as below:

$$\frac{\Delta V_{out}}{\Delta I_{out}} = \begin{cases} \dfrac{R_{out}}{2(1+s\cdot\dfrac{R_{out}C_{out}}{2})} & \text{Resistive Load} \\ \dfrac{1}{sC_{out}} & \text{Constant Power Load} \end{cases} \quad (45)$$

In this application note, the calculation is only carried out for constant power load situation

3.3.1.2 ΔI_{out} / ΔI_{L_rms}

The current source Iout can be characterized with the following considerations as shown in Figure 21. The low frequency component of the boost diode current is found by averaging the discharge portion of the inductor current over a given switching cycle. The low frequency current, averaged over a mains half-cycle yields the DC output current Iout:

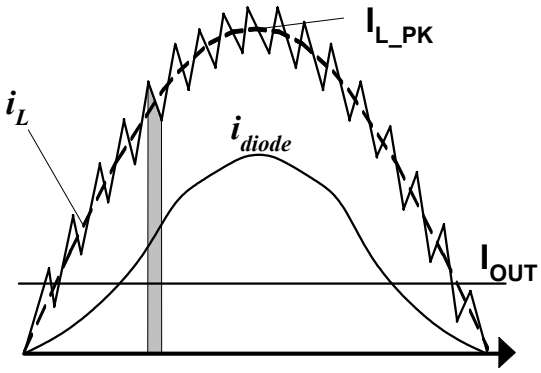


Figure 21 The simplification and characterization for I_{out} / I_{L_rms}

$$I_{out} = \frac{1}{\pi}\int_0^{\pi}(1-D_{on})I_{L\_PK}Sin\alpha d\alpha = \frac{2V_{inrms}I_{L\_rms}}{\pi V_{out\_AVE}}\int_0^{\pi}(Sin\alpha)^2 d\alpha = \frac{V_{inrms}I_{L\_rms}}{V_{out\_AVE}} \quad (46)$$

So,

$$\frac{\Delta I_{out}}{\Delta I_{L\_rms}} = \frac{V_{inrms}}{V_{out\_AVE}} \quad (47)$$

where, Don is the switch duty cycle; α is the instantaneous phase angle of the mains voltage, Vinrms is the input RMS voltage value, I_{L_PK} is choke current sinewave peak value and V_{out_AVE} is the averaging bulk DC output voltage.

In case of constant power load, the transfer function of $G_3(s)$ is:

$$G_3(s) = \frac{\Delta V_{out}}{\Delta I_{L\_rms}} = \frac{\Delta V_{out}}{\Delta I_{out}}\cdot\frac{\Delta I_{out}}{\Delta I_{L\_rms}} = \frac{V_{inrms}}{V_{out\_AVE}}\cdot\frac{1}{sC_{out}} \quad (48)$$

3.3.2 Small signal transfer function of $\Delta V_{out}/\Delta(M_1M_2)$ for voltage loop analysis

There is a internal feedback from Vout to $G_2(s)$. this inner loop has to be solved to obtain the transfer function of $\Delta V_{out}/\Delta$(M1M2). Rewrite the equation (43) at input voltage RMS point:

$$I_{L\_rms} = \frac{K_{FQ}M_1M_2V_{inrms}}{K_1R_{sense}V_{out}} \quad (49)$$

making a perturbation on I_{L_rms}, (M_1M_2), V_{out}, then

$$\Delta I_{L\_rms} = \frac{I_{L\_rms}}{M_1 M_2}\Delta(M_1 M_2) - \frac{I_{L\_rms}}{V_{out\_AVE}}\Delta V_{out} \tag{50}$$

replacing ΔI_{L_rms} by $\Delta V_{out}/G_3(s)$ according to voltage loop block diagram,

$$\frac{\Delta V_{out}}{G_3(s)} = \frac{I_{L\_rms}}{M_1 M_2}\Delta(M_1 M_2) - \frac{I_{L\_rms}}{V_{out\_AVE}}\Delta V_{out} \tag{51}$$

then the transfer function of dV_{out}/dV_{comp} is

$$G_{23}(s) = \frac{\Delta V_{out}}{\Delta(M_1 M_2)} = \frac{\frac{V_{out\_AVE}}{M_1 M_2}}{\frac{V_{out\_AVE}^{\ 2} C_{out}}{I_{L\_rms} V_{inrms}}s + 1} = \frac{\frac{V_{out\_AVE}}{M_1 M_2}}{\frac{K_1 R_{sense} V_{out\_AVE}^{\ 3} C_{out}}{K_{FQ} M_1 M_2 V_{inrms}^{\ 2}}s + 1} \tag{52}$$

With $f_{23} = \dfrac{1}{2\pi \dfrac{K_1 R_{sense} V_{out\_AVE}^{\ 3} C_{out}}{K_{FQ} M_1 M_2 V_{inrms}^{\ 2}}}$,

$$G_{23}(s) = \frac{\Delta V_{out}}{\Delta(M_1 M_2)} = \frac{\frac{V_{out\_AVE}}{M_1 M_2}}{1 + \frac{s}{2\pi f_{23}}} \tag{53}$$

3.3.3 Nonlinear block $G_{NON}(s)$

The Vcomp voltage is sent to nonlinear gain block. The output of nonlinear is two internal variables, M1 and M2. The two variables are used to define boost choke current amplitude I_L as in equation (43). The characteristic of nonlinear gain block is shown in Table 2 and Figure 22. The small signal gain between Δ(M1*M2) and ΔVcomp can be derived as well at different operating point.

Vcomp	M1	M2	M1*M2
0.00	4.686E-02	4.964E-04	2.326E-05
0.25	4.685E-02	7.072E-04	3.313E-05
0.50	4.665E-02	1.199E-03	5.595E-05
0.75	4.685E-02	3.292E-03	1.542E-04
1.00	4.823E-02	3.224E-02	1.555E-03
1.25	8.153E-02	1.075E-01	8.766E-03
1.50	1.261E-01	1.921E-01	2.423E-02
1.75	1.901E-01	2.796E-01	5.316E-02
2.00	2.747E-01	3.686E-01	1.013E-01
2.25	3.768E-01	4.590E-01	1.729E-01
2.50	4.884E-01	5.523E-01	2.697E-01
2.75	5.992E-01	6.539E-01	3.918E-01
3.00	6.992E-01	7.794E-01	5.449E-01
3.25	7.816E-01	9.669E-01	7.557E-01
3.50	8.443E-01	1.287E+00	1.087E+00
3.75	8.888E-01	1.802E+00	1.601E+00
4.00	9.184E-01	2.442E+00	2.243E+00
4.25	9.339E-01	2.911E+00	2.719E+00

4.50	9.350E-01	2.911E+00	2.722E+00
4.75	9.351E-01	2.911E+00	2.722E+00
5.00	9.351E-01	2.911E+00	2.722E+00

Table 2 nonlinear block characteristic data

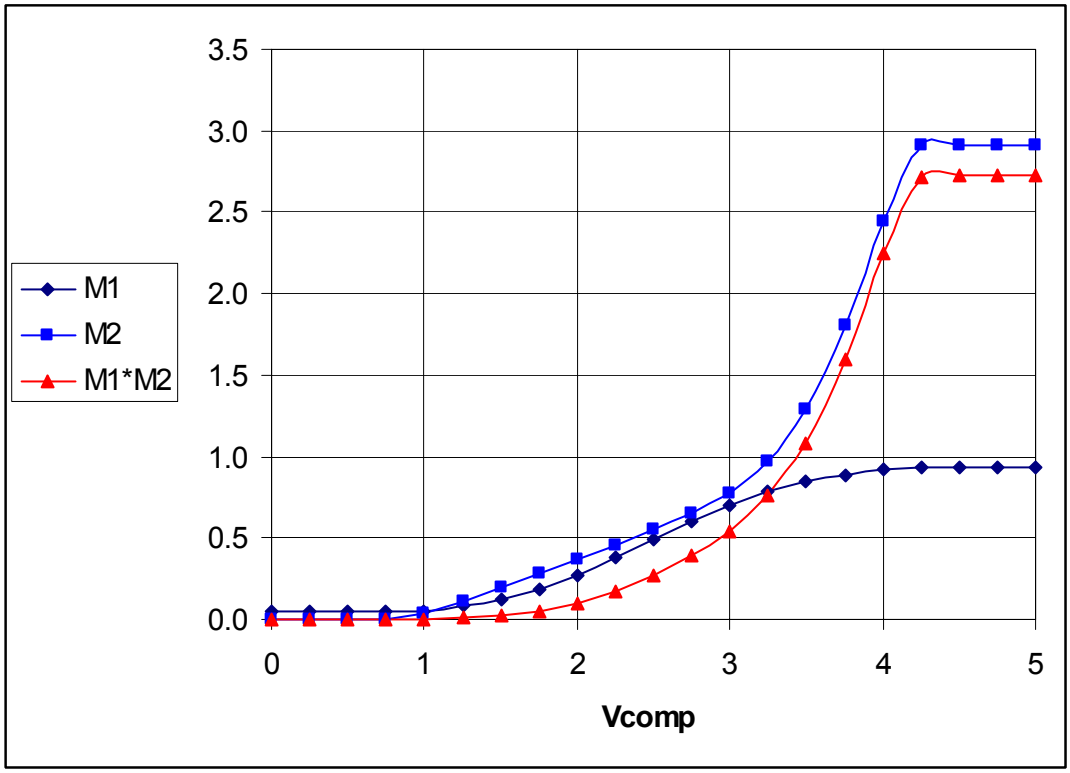


Figure 22 The characteristics of nonlinear block

3.3.4 Error Amplifier compensation $G_1(s)$

The circuit of error amplifier compensation circuit is shown in Figure 23. The sensing voltage Vsense is compared to internal reference voltage 3V typical. The difference between Vsense and internal reference is sent to transconductance error amplifier and converted to a current source to charge or discharge the RC components in Vcomp Pin.

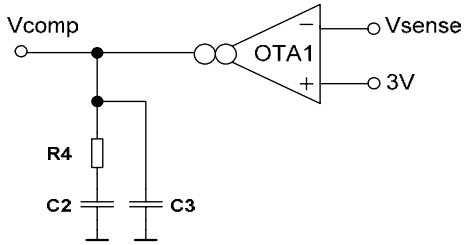


Figure 23 Error Amplifier compensation $G_1(s)$

The transfer function is:

$$G_1(s) = \frac{\Delta V_{comp}}{\Delta V_{sense}} = \frac{\Delta V_{comp}}{\Delta I_{OTA1}} \cdot \frac{\Delta I_{OTA1}}{\Delta V_{sense}} = \frac{1 + sR_4C_2}{(C_2 + C_3)s(1 + s\frac{R_4C_2C_3}{C_2 + C_3})} \cdot g_{OTA1} \quad (54)$$

where, g_{OTA1} is the trans-conductance of OTA1, 42uS typically for ICE2PCS02.

With $f_{CZ} = \frac{1}{2\pi R_4 C_2}$ and $f_{CP} = \frac{1}{2\pi \frac{R_4 C_2 C_3}{C_2 + C_3}}$,

$$G_1(s) = \frac{g_{OTA1}(1 + s/2\pi f_{CZ})}{(C_2 + C_3)s(1 + s/2\pi f_{CP})} \quad (55)$$

The pole and zero are to regulate the overall voltage loop with the cross-over frequency below 100Hz and create the phase margin for the loop stability.

3.3.5 Feedback $G_4(s)$

The Feedback block is a simple voltage divider to monitor the bulk capacitor output voltage. The circuit is shown in Figure 24.

$$G_4(s) = \frac{\Delta V_{sense}}{\Delta V_{out}} = \frac{R_2}{R_1 + R_2} \quad (56)$$

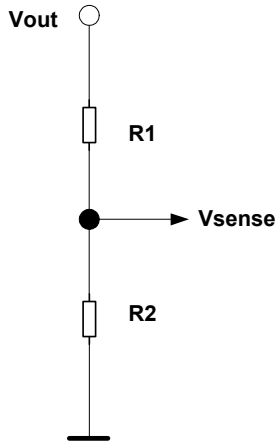


Figure 24 bulk voltage sensing divider

3.3.6 Overall Open Loop Transfer Function $G_V(s)$

With combining all of the blocks above, the overall open loop gain for voltage loop is equal to:

$$G_V(s) = G_1(s)G_{NON}(s)G_{23}(s)G_4(s) \quad (57)$$

Due to PF requirement, inherent PFC dynamic voltage loop compensation is always implemented with low bandwidth in order not to make the response for $2*f_L$ ripple. For example, for 50Hz AC line input, PFC voltage loop bandwidth is normally set below 20Hz. The compensation circuit R4, C2 and C3 are used to optimize the loop gain and phase margin.

3.3.7 Enhance dynamic response

As mentioned in Section 4.6, the inherent low bandwidth of voltage loop in PFC application will lead to slow response in case of sudden load step and result in large output overshoot or drop. Enhance dynamic response feature is integrated in ICE2PCS02 to have a fast response in the case of load step. The voltage loop with including enhance dynamic response block is shown in Figure 25.

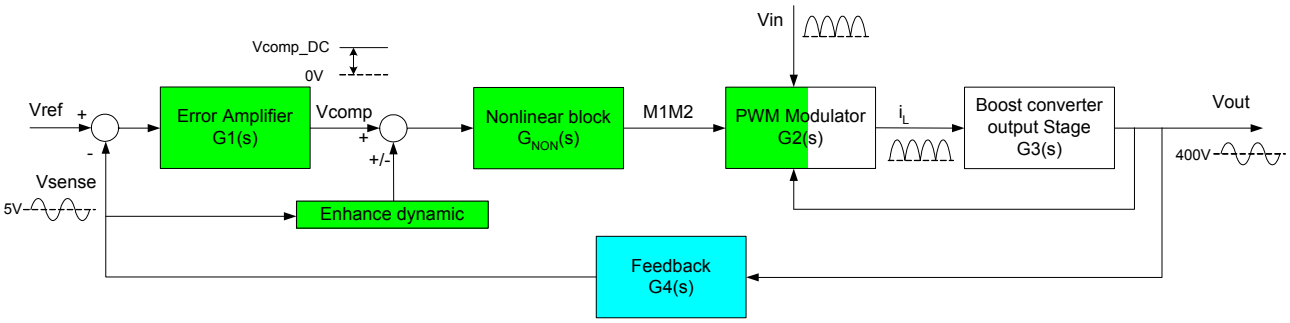


Figure 25 voltage loop block diagram including enhance dynamic response

When Vsense voltage variation is within -5% to +5% of nominal value, there is no function of enhance dynamic response block. However, when Vsense variation is out of such +/-5% range, enhance block will add offset voltage on top of Vcomp voltage to influence the current amplitude.

The timing diagram of enhance dynamic response operation is shown in Figure 26 with sudden load jump situation. It can be seen that during enhance dynamic operation, the high current of boost choke is delivered for fast response. Within half sinusoidal period, when Vsense operating around the boundary of -5% threshold, the first part of boost choke current follows high amplitude profile due to enhance mode offset and the rest of boost choke current come back to low amplitude profile without enhance mode offset. When Vsense voltage is pulled back within +/-5% range, enhance dynamic offset disappear and boost choke current waveform will stay as perfect sinusoidal shape.

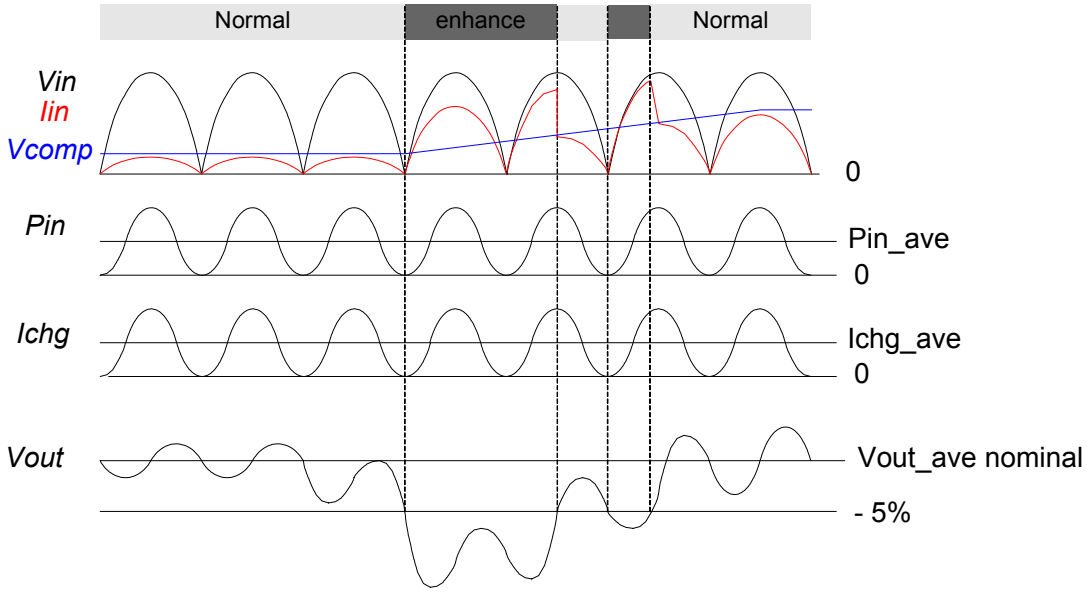


Figure 26 timing diagram for enhance dynamic operation

3.4 Design Example

Assuming a 300W application with universal input AC voltage 85~265VAC,

constant power load
efficiency=90%

Vout=400VDC
Cout=220uF/450V
f_{SW}=125kHz
Rsense=0.1ohm
Boost choke inductance L=1.2mH (please note that the inductance may change at different choke current)
Vsense divider: R1=390kohm*2=780kohm, R2=6kohm

3.5 Vcomp and M1, M2 value at full load condition

(1) 85VAC:

RMS AC input current under full load:

$$I_{L\_rms\_85} = \frac{P_{out}}{\eta \cdot V_{inrms\_85}} = \frac{300}{0.9 \cdot 85} = 3.92A \tag{58}$$

From equation (43), With $K_{FQ} = 4.34$ and $K_1 = 4$ from the ICE2PCS02 Datasheet,

$$M_1 M_2\big|_{85VAC} = \frac{I_{L\_rms\_85} K_1 R_{sense} V_{out}}{K_{FQ} V_{inrms\_85}} = \frac{3.92 \cdot 4 \cdot 0.1 \cdot 400}{4.34 \cdot 85} = 1.70 \tag{59}$$

From table 2 and Figure 22, it can be obtained

Vcomp	M1	M2	M1*M2
3.75	8.888E-01	1.802E+00	1.601E+00
4.00	9.184E-01	2.442E+00	2.243E+00

With Linear approximation:

$$V_{comp\_85} = V_{comp\_1} + \frac{M_1 M_2\big|_{85VAC} - M_1 M_2\big|_{Vcomp\_1}}{M_1 M_2\big|_{Vcomp\_2} - M_1 M_2\big|_{Vcomp\_1}} \cdot (V_{comp\_2} - V_{comp\_1}) \tag{60}$$

$$V_{comp\_85} = 3.75 + \frac{1.70 - 1.601}{2.243 - 1.601} \cdot (4 - 3.75) = 3.79V$$

$$M_1\big|_{85VAC} = M_{1\_1} + \frac{M_{1\_2} - M_{1\_1}}{V_{comp\_2} - V_{comp\_1}} \cdot (V_{comp\_85} - V_{comp\_1}) \tag{61}$$

$$M_1\big|_{85VAC} = 0.889 + \frac{0.918 - 0.889}{4 - 3.75} \cdot (3.79 - 3.75) = 0.894$$

$$M_2\big|_{85VAC} = M_{2\_1} + \frac{M_{2\_2} - M_{2\_1}}{V_{comp\_2} - V_{comp\_1}} \cdot (V_{comp\_85} - V_{comp\_1}) \tag{62}$$

$$M_2\big|_{85VAC} = 1.802 + \frac{2.442 - 1.802}{4 - 3.75} \cdot (3.79 - 3.75) = 1.91$$

The small signal gain of nonlinear block is

$$G_{NON}(s)\big|_{85VAC} = \frac{M_1 M_2\big|_{Vcomp\_2} - M_1 M_2\big|_{Vcomp\_1}}{V_{comp\_2} - V_{comp\_1}} = \frac{2.243 - 1.601}{4 - 3.75} = 2.568 \tag{63}$$

The inherent pole of f_{23} is

$$f_{23}\big|_{85VAC} = \frac{1}{2\pi \frac{K_1 R_{sense} V_{out\_AVE}{}^3 C_{out}}{K_{FQ} \cdot (M_1 M_2)\big|_{85VAC} \cdot V_{inrms\_85}{}^2}} = 1.54Hz \quad (64)$$

(2) 265VAC

RMS AC input current under full load:

$$I_{L\_rms\_265} = \frac{P_{out}}{\eta \cdot V_{inrms\_265}} = \frac{300}{0.9 \cdot 265} = 1.257A \quad (65)$$

From equation (43),

$$M_1 M_2\big|_{265VAC} = \frac{I_{L\_rms\_265} K_1 R_{sense} V_{out}}{K_{FQ} V_{inrms\_265}} = \frac{1.257 \cdot 4 \cdot 0.1 \cdot 400}{4.34 \cdot 265} = 0.175 \quad (66)$$

From table 2 and Figure 22, it can be obtained

Vcomp	M1	M2	M1*M2
2.25	3.768E-01	4.590E-01	1.729E-01
2.50	4.884E-01	5.523E-01	2.697E-01

With Linear approximation:

$$V_{comp\_265} = V_{comp\_1} + \frac{M_1 M_2\big|_{265VAC} - M_1 M_2\big|_{Vcomp\_1}}{M_1 M_2\big|_{Vcomp\_2} - M_1 M_2\big|_{Vcomp\_1}} \cdot (V_{comp\_2} - V_{comp\_1})$$

$$V_{comp\_265} = 2.25 + \frac{0.175 - 0.1729}{0.2697 - 0.1729} \cdot (2.5 - 2.25) = 2.255V \quad (67)$$

$$M_1\big|_{265VAC} = M_{1\_1} + \frac{M_{1\_2} - M_{1\_1}}{V_{comp\_2} - V_{comp\_1}} \cdot (V_{comp\_265} - V_{comp\_1})$$

$$M_1\big|_{265VAC} = 0.3768 + \frac{0.4884 - 0.3768}{2.5 - 2.25} \cdot (2.266 - 2.25) = 0.386 \quad (68)$$

$$M_2\big|_{265VAC} = M_{2\_1} + \frac{M_{2\_2} - M_{2\_1}}{V_{comp\_2} - V_{comp\_1}} \cdot (V_{comp\_265} - V_{comp\_1})$$

$$M_2\big|_{265VAC} = 0.459 + \frac{0.5523 - 0.459}{2.5 - 2.25} \cdot (2.255 - 2.25) = 0.461 \quad (69)$$

The small signal gain of nonlinear block is

$$G_{NON}(s)\big|_{265VAC} = \frac{M_1 M_2\big|_{Vcomp\_2} - M_1 M_2\big|_{Vcomp\_1}}{V_{comp\_2} - V_{comp\_1}} = \frac{0.2697 - 0.1729}{2.5 - 2.25} = 0.3872 \quad (70)$$

The inherent pole of f_{23} is

$$f_{23}\big|_{265VAC} = \frac{1}{2\pi \frac{K_1 R_{sense} V_{out\_AVE}{}^3 C_{out}}{K_{FQ} \cdot (M_1 M_2)\big|_{265VAC} \cdot V_{inrms\_265}{}^2}} = 1.54Hz \quad (71)$$

3.5.1 Current Averaging Circuit

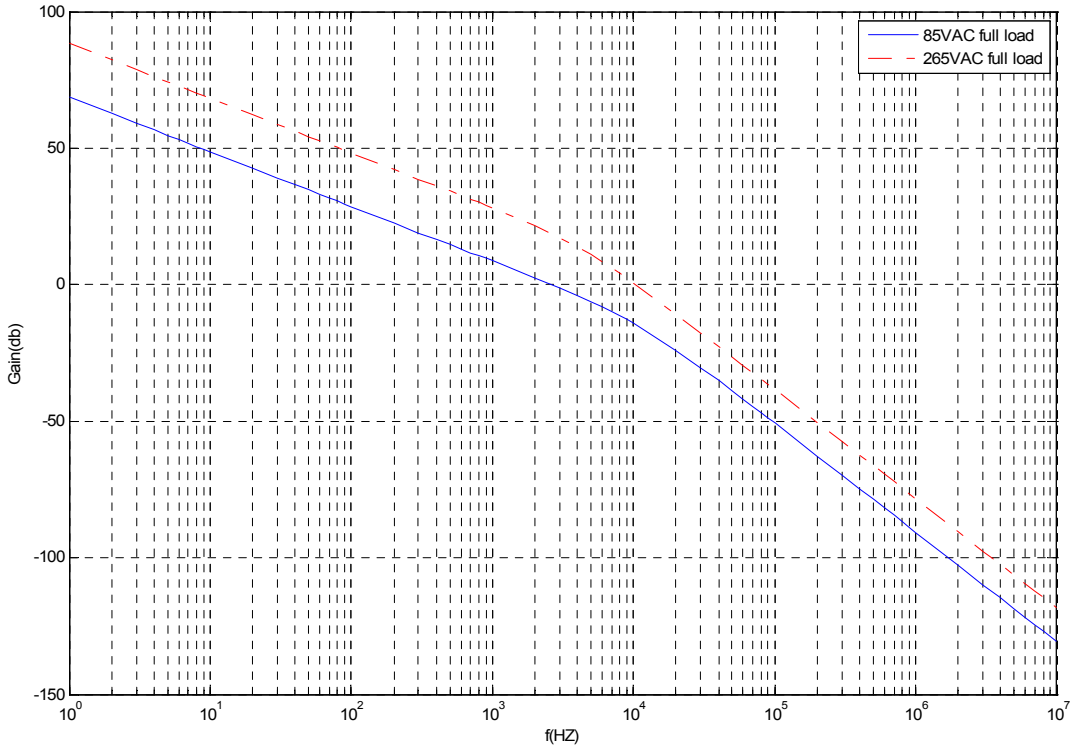
With g_{OTA2}=1.0mS from Datasheet, M1@85VAC, and assuming f_{AVE}=13kHz which is 10 times less than switching frequency 125kHz, then

$$C_{icomp} \geq \frac{g_{OTA2} M_1\big|_{85VAC}}{K_1 \cdot 2\pi f_{AVE}} = \frac{1.0E-3 \cdot 0.895}{4 \cdot 2\pi \cdot 24E3} = 3nF \tag{72}$$

Select C_{icomp}=3.3nF

3.5.2 Current Loop Regulation

Insert M1 and M2 value in equation (40). The amplitude and phase angle of $G_C(s)$ is shown in Figure 27 to verify the stability of current loop and the requirement of f_C less than switching frequency.



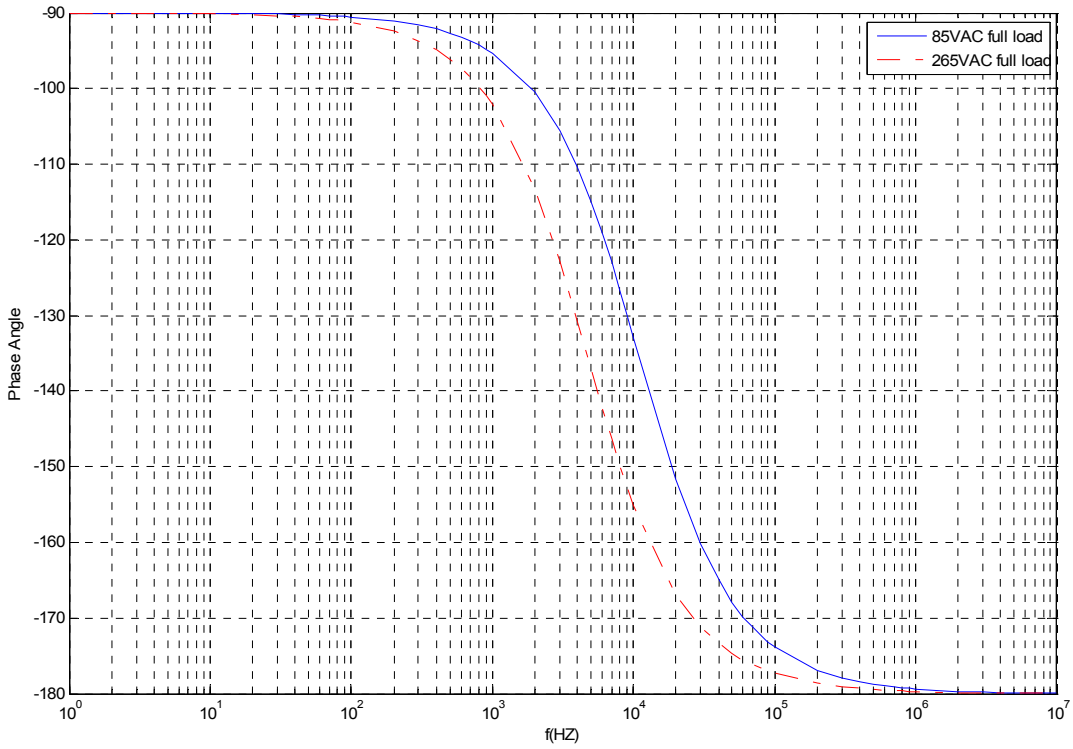


Figure 27 The bode plot and phase angle for current loop

The cross over frequency and phase margin are 3kHz and 75º for 85VAC, and 10kHz and 25º for 265VAC.

3.5.3 Voltage Loop Regulation

From the above sections, it can be obtained:

$$G_1(s) = \frac{\Delta V_{comp}}{\Delta V_{sense}} = \frac{g_{OTA1}(1 + s/2\pi f_{CZ})}{(C_2 + C_3)s(1 + s/2\pi f_{CP})} \tag{73}$$

$$G_{NON}(s) = \frac{\Delta(M_1 M_2)}{\Delta V_{comp}} \tag{74}$$

$$G_{23}(s) = \frac{\Delta V_{out}}{\Delta(M_1 M_2)} = \frac{\frac{V_{out\_AVE}}{M_1 M_2}}{1 + \frac{s}{2\pi f_{23}}} \tag{75}$$

$$G_4(s) = \frac{\Delta V_{sense}}{\Delta V_{out}} = \frac{R_2}{R_1 + R_2} = \frac{6.2}{806.2}. = 0.0077 \tag{76}$$

The open loop gain for voltage loop is to times all above factors together as:

$$G_V(s) = G_1(s) G_{NON}(s) G_{23}(s) G_4(s)$$

$G_1(s)$ is used to provide enough phase margin and also limit the bandwidth below 20HZ. R4, C2 and C3 can be chosen as required. f_{CZ} normally select to be compensate the pole in $G_{23}(s)$. f_{CP} normally select to be 40~70Hz in order to fast put down the gain amplitude and reject the high frequency interference. In this example f_{23} is around 1.54Hz at 85VAC/ 265VAC and full load. So the initial target is: f_{CZ} is chosen to be close to 1.5Hz, and f_{CP} is chosen to be 50Hz.

C2 and C3 is calculated to obtain Gv(s) cross over frequency around 10Hz. The gain amplitude of G_{NON}*G_{23}*G_4 in 85VAC and full load is shown in Figure 28. It can be seen that at f=10Hz, the gain is about -4.52dB. So G1 should provide the gain +4.52dB at f=10Hz. Considering that C2>>C3 due to fcz<fcp and 10Hz>>1Hz=f_{CZ}, then

$$G_1(10Hz) = \frac{g_{OTA1} \, 10Hz/1Hz}{C_2 \cdot 2\pi \cdot 10Hz} = +4.52dB$$
$$C_2 = \frac{39 \cdot 10^{-6} \cdot \frac{10Hz}{1Hz}}{10^{4.52/20} \cdot 2\pi \cdot 10Hz} = 3.69\mu F \tag{77}$$

3.97uF is not common for ceramic type capacitor. So select C_2=1uF, then f_{CZ} is recalculated as:

$$G_1(10Hz) = \frac{g_{OTA1}\sqrt{1+(10Hz/f_{CZ})^2}}{C_2 \cdot 2\pi \cdot 10Hz} = +4.52dB$$

$$f_{CZ} = \frac{10Hz}{\sqrt{\left(\frac{1\mu F \cdot 10^{4.52/20} \cdot 2\pi \cdot 10Hz}{39 \cdot 10^{-6}}\right)^2 - 1}} = 4.30Hz \quad (78)$$

according to $f_{CZ} = \frac{1}{2\pi R_4 C_2} = 4.30Hz$ then

$$R_4 = \frac{1}{2\pi \cdot 4.30Hz \cdot C_2} = 37k\Omega \quad (79)$$

select R4=33kΩ, and $f_{CP} = \frac{1}{2\pi \frac{R_4 C_2 C_3}{C_2 + C_3}} \approx \frac{1}{2\pi R_4 C_3} = 50Hz$

$$C_3 = \frac{1}{2\pi \cdot 50Hz \cdot R_4} = 96.5nF \quad (80)$$

select C3=100nF

The gain amplitude and phase angle of overall voltage loop $G_V(s)$ at 85VAC and 265VAC in full load condition is shown in Figure 28 and Figure 29. At 85VAC, the cross over frequency f_V is around 9.5Hz and the phase margin is about 63º. At 265VAC, the cross over frequency f_V is around 14Hz and the phase margin is about 62º.

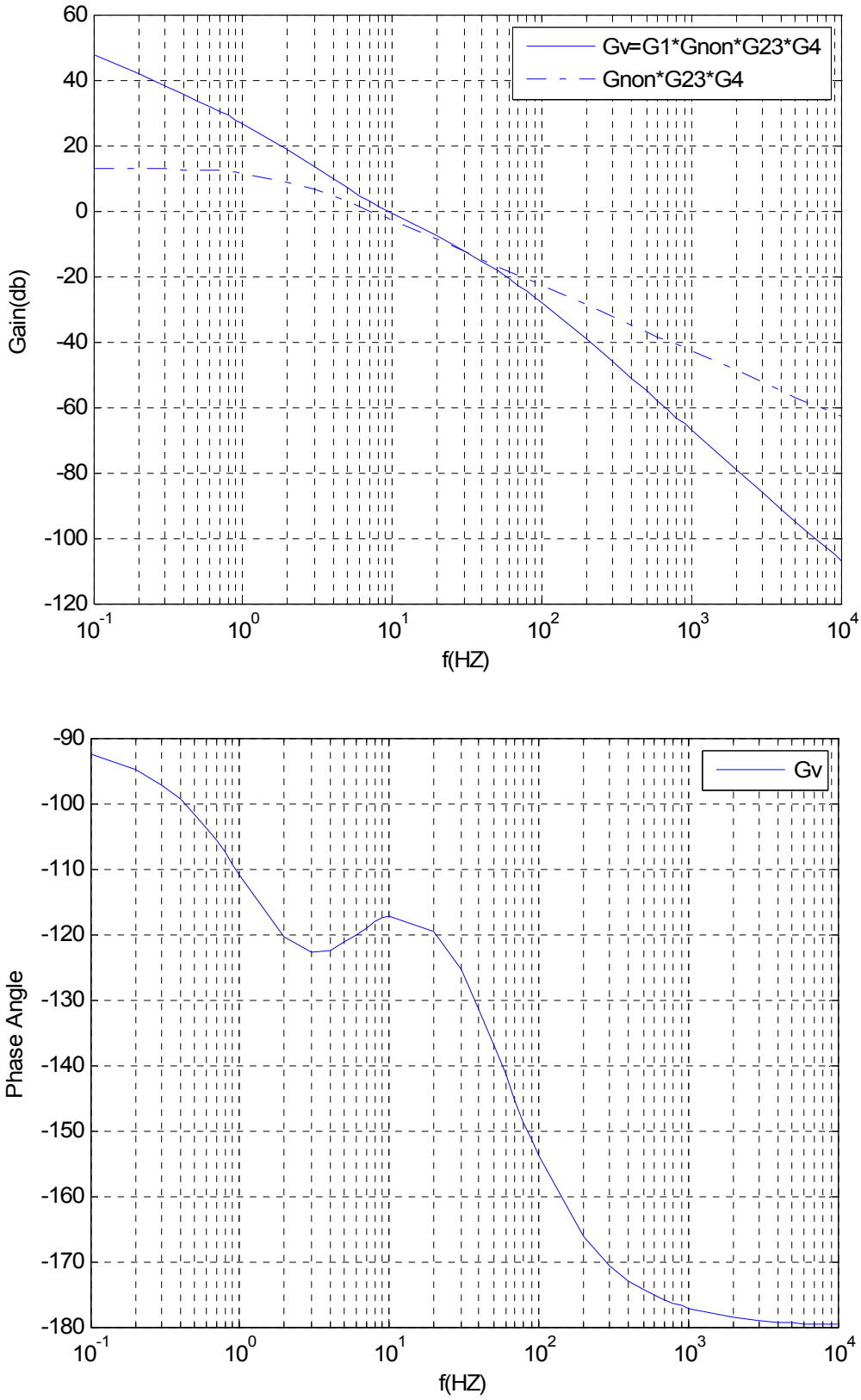


Figure 28 the bode plot and phase angle for voltage loop at 85VAC and full load

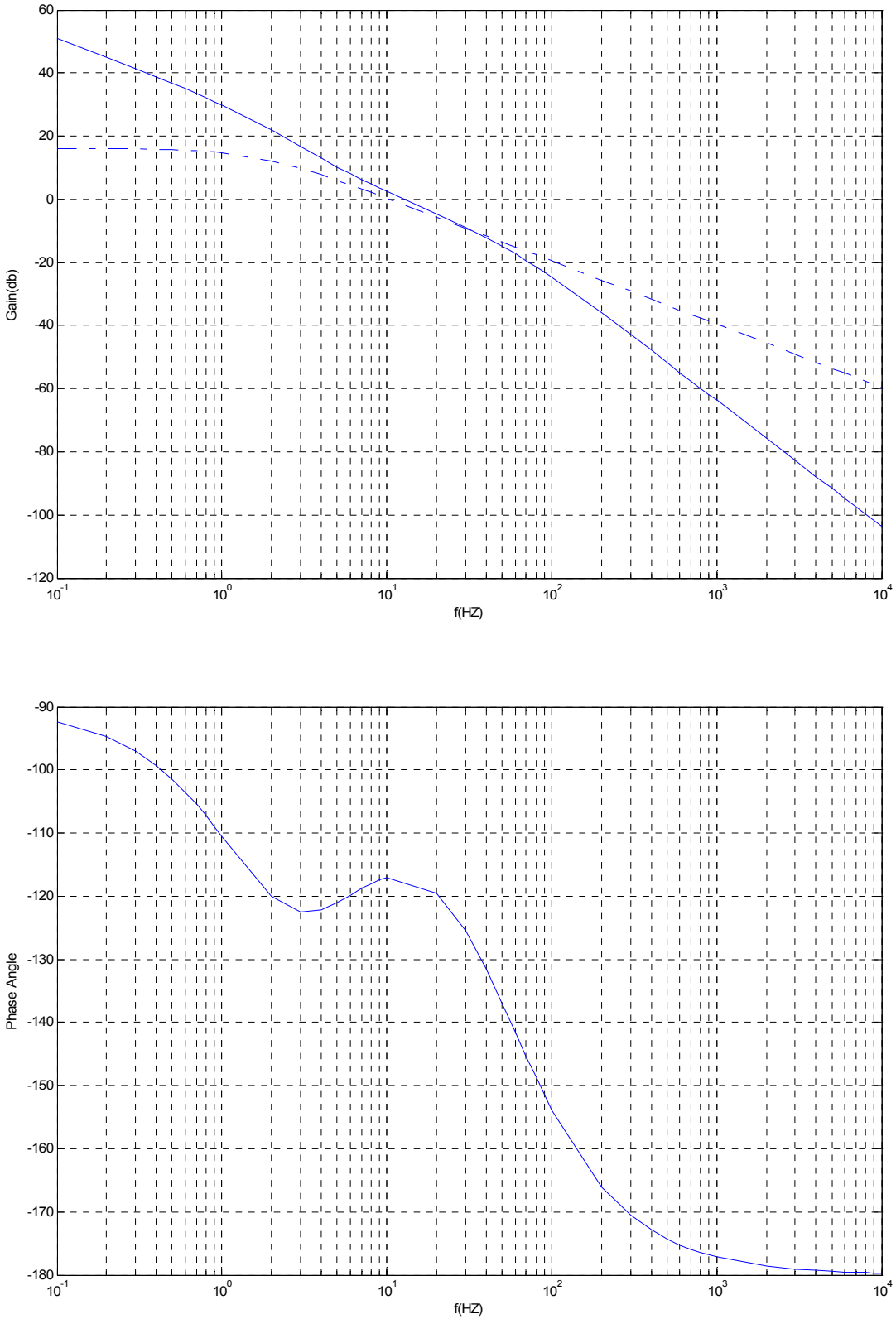


Figure 29 The bode plot and phase angle for voltage loop at 265VAC and full load

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Application Note AN4134

Design Guidelines for Off-line Forward Converters Using Fairchild Power Switch (FPS™)

Abstract

This paper presents practical design guidelines for off-line forward converter employing FPS (Fairchild Power Switch). Switched mode power supply (SMPS) design is inherently a time consuming job requiring many trade-offs and iteration with a large number of design variables.
The step-by-step design procedure described in this paper helps the engineers to design a SMPS easily. In order to make the design process more efficient, a software design tool, **FPS design assistant,** that contains all the equations described in this paper, is also provided.

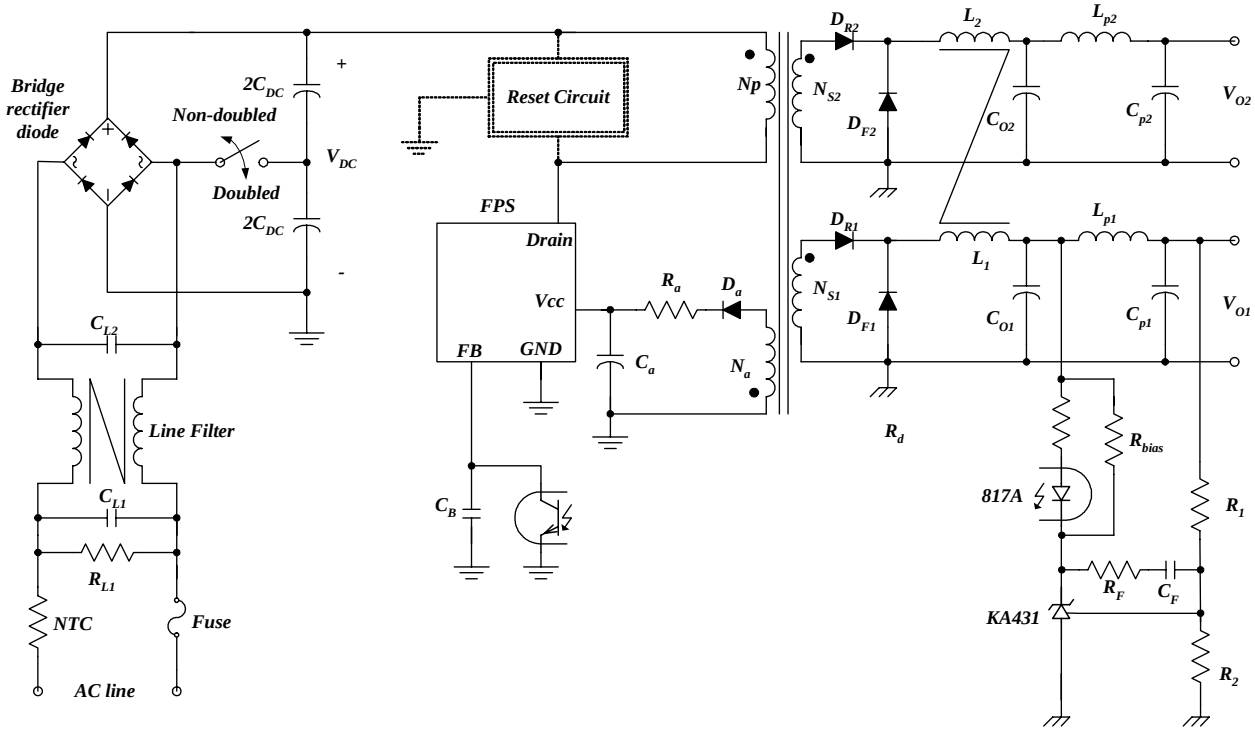


Figure 1. Basic Off-line Forward Converter Using FPS

1. Introduction

Due to circuit simplicity, the forward converter has been widely used for low to medium power conversion applications. Figure 1 shows the schematic of the basic off-line forward converter using FPS, which also serves as the reference circuit for the design procedure described in this paper. Because the MOSFET and PWM controller together with various additional circuits are integrated into a single package, the design of SMPS is much easier than the discrete MOSFET and PWM controller solution.

This paper provides step-by-step design procedure for an FPS based off-line forward converter, which includes transformer design, reset circuit design, output filter design, component selection and closing the feedback loop. The design procedure described herein is general enough to be applied to various applications. The design procedure presented in this paper is also implemented in a software design tool (FPS design assistant) to enable the engineer to finish SMPS design in a short time. In the appendix, a step-by-step design example using the software tool is provided.

2. Step-by-step Design Procedure

In this section, design procedure is presented using the schematic of the figure 1 as a reference. In general, most FPS has the same pin configuration from pin 1 to pin 4, as shown in figure 1.

(1) STEP-1 : Determine the system specifications

- Line voltage range (V_{line}^{min} and V_{line}^{max}) : Usually, voltage doubler circuit as shown in figure 1 is used for a forward converter with universal input. Then, the minimum line voltage is twice the actual minimum line voltage.

- Line frequency (f_L).

- Maximum output power (P_o).

- Estimated efficiency (E_{ff}) : It is required to estimate the power conversion efficiency to calculate the maximum input power. If no reference data is available, set E_{ff} = 0.7~0.75 for low voltage output applications and E_{ff} = 0.8~0.85 for high voltage output applications.

With the estimated efficiency, the maximum input power is given by

$$P_{in} = \frac{P_o}{E_{ff}} \qquad (1)$$

Considering the maximum input power, choose the proper FPS. Since the voltage stress on the MOSFET is about twice the input voltage in the case of the forward converter, an FPS with 800V rated MOSFET is recommended for universal input voltage. The FPS lineup with proper power rating is also included in the software design tool.

(2) STEP-2 : Determine DC link capacitor (C_{DC}) and the DC link voltage range.

The maximum DC link voltage ripple is obtained as

$$\Delta V_{DC}^{max} = \frac{P_{in} \cdot (1 - D_{ch})}{\sqrt{2} V_{line}^{min} \cdot 2f_L \cdot C_{DC}} \qquad (2)$$

where D_{ch} is the DC link capacitor charging duty ratio defined as shown in figure 2, which is typically about 0.2.

It is typical to set ΔV_{DC}^{max} as 10~15% of $\sqrt{2} V_{line}^{min}$ For voltage doubler circuit, two capacitors are used in series, each of which has capacitance twice of the capacitance that is determined by equation (2).

With the resulting maximum voltage ripple, the minimum and maximum DC link voltages are given as

$$V_{DC}^{min} = \sqrt{2} V_{line}^{min} - \Delta V_{DC}^{max} \qquad (3)$$

$$V_{DC}^{max} = \sqrt{2} V_{line}^{max} \qquad (4)$$

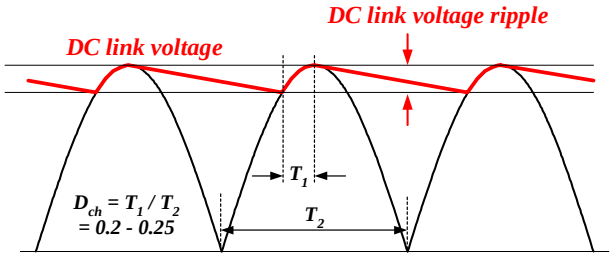


Figure 2.DC Link Voltage Waveform

(3) STEP-3 : Determine the transformer reset method and the maximum duty ratio (D_{max})

One inherent limitation of the forward converter is that the transformer must be reset during the MOSFET off period. Thus, additional reset schemes should be employed. Two most commonly used reset schemes are auxiliary winding reset and RCD reset. According to the reset schemes, the design procedure is changed a little bit.

(a) <u>Auxiliary winding reset</u> : Figure 3 shows the basic circuit diagram of forward converter with auxiliary winding reset. This scheme is advantageous in respect of efficiency since the energy stored in the magnetizing inductor goes back to the input. However, the extra reset winding makes the construction of the transformer more complicated.

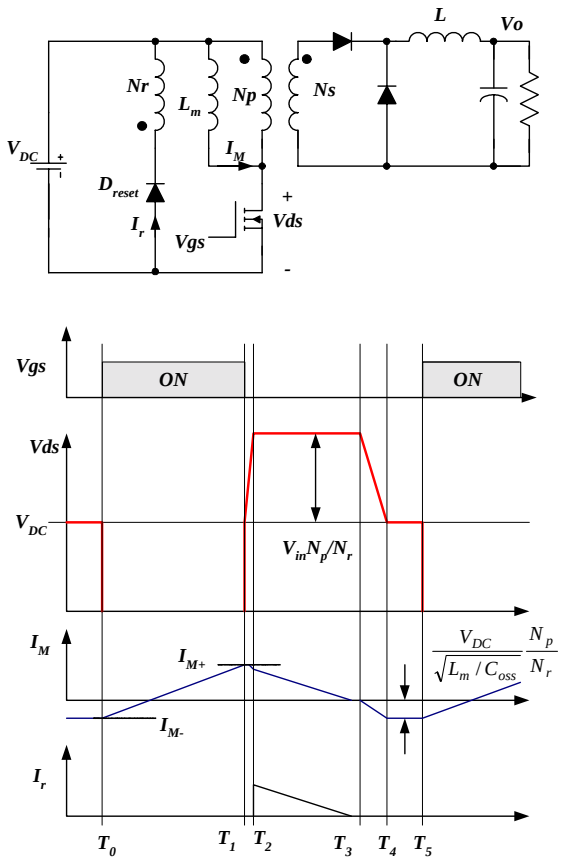


Figure 3. Auxiliary Winding Reset Forward Converter

The maximum voltage on MOSFET and the maximum duty ratio are given by

$$V_{ds}^{max} = V_{DC}^{max}\left(1+\frac{N_p}{N_r}\right) \quad (5)$$

$$D_{max} \le \frac{N_p}{N_p+N_r} \quad (6)$$

where N_p and N_r are the number of turns for the primary winding and reset winding, respectively.

As can be seen in equations (5) and (6), the maximum voltage on the MOSFET can be reduced by decreasing D_{max}. However, decreasing D_{max} results in increased voltage stress on the secondary side. Therefore, it is proper to set D_{max}=0.45 and N_p=N_r for universal input. For auxiliary winding reset, FPS, of which duty ratio is internally limited below 50%, is recommended to prevent core saturation during transient.

(b) <u>RCD reset</u> : Figure 4 shows the basic circuit diagram of the forward converter with RCD reset. One disadvantage of this scheme is that the energy stored in the magnetizing inductor is dissipated in the RCD snubber, unlike in the reset winding method. However, due to its simplicity, this scheme is widely used for many cost-sensitive SMPS.

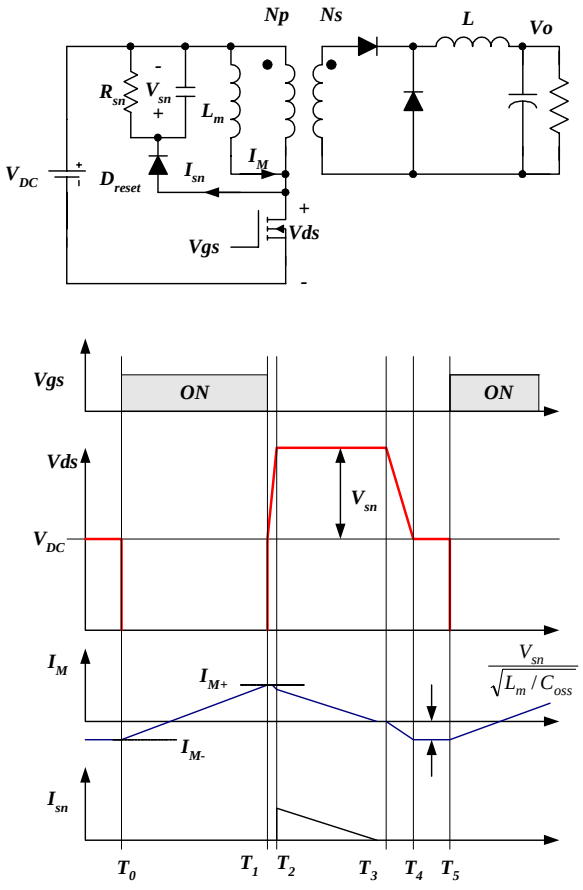


Figure 4. RCD Reset Forward Converter

The maximum voltage stress and the nominal snubber capacitor voltage are given by

$$V_{ds}^{max} = V_{DC}^{max} + V_{sn} \quad (7)$$

$$V_{sn} > \frac{V_{DC}^{min} \cdot D_{max}}{(1-D_{max})} \quad (8)$$

Since the snubber capacitor voltage is fixed and almost independent of the input voltage, the MOSFET voltage stress can be reduced compared to the reset winding approach when the converter is operated with a wide input voltage range. Another advantage of RCD reset method is that it is possible to set the maximum duty ratio larger than 50% with relatively low voltage stress on the MOSFET compared to auxiliary winding reset method, which results in reduced voltage stress on the secondary side.

(4) STEP-4 : Determine the ripple factor of the output inductor current.

Figure 5 shows the current of the output inductor. The ripple factor is defined as

$$K_{RF} = \frac{\Delta I}{2I_o} \quad (9)$$

where I_o is the maximum output current. For most practical design, it is reasonable to set K_{RF}=0.1~ 0.2.

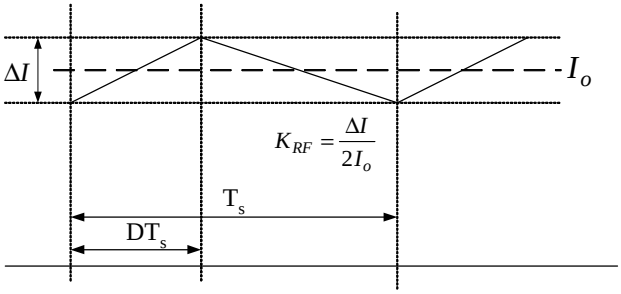


Figure 5. Output Inductor Current and Ripple Factor

Once the ripple factor is determined, the peak current and rms current of MOSFET are obtained as

$$I_{ds}^{peak} = I_{EDC}(1+K_{RF}) \quad (10)$$

$$I_{ds}^{rms} = I_{EDC}\sqrt{(3+K_{RF}^2)\frac{D_{max}}{3}} \quad (11)$$

$$where \qquad I_{EDC} = \frac{P_{in}}{V_{DC}^{min} \cdot D_{max}} \quad (12)$$

Check if the MOSFET maximum peak current (I_{ds}^{peak}) is below the pulse-by-pulse current limit level of the FPS (I_{lim}).

(5) STEP-5 : Determine the proper core and the minimum primary turns for the transformer to prevent core saturation.

Actually, the initial selection of the core is bound to be crude since there are too many variables. One way to select the proper core is to refer to the manufacture's core selection guide. If there is no proper reference, use the following equation as a starting point.

$$A_p = A_w A_e = \left[\frac{11.1 \times P_{in}}{0.141 \cdot \Delta B \cdot f_s}\right]^{1.31} \times 10^4 (mm^4) \quad (13)$$

where A_w is the window area and A_e is the cross sectional area of the core in mm^2 as shown in figure 6. f_s is the switching frequency and ΔB is the maximum flux density swing in tesla for normal operation. ΔB is typically 0.2-0.3 T for most power ferrite cores in the case of a forward converter. Notice that the maximum flux density swing is small compared to flyback converter due to the remnant flux density.

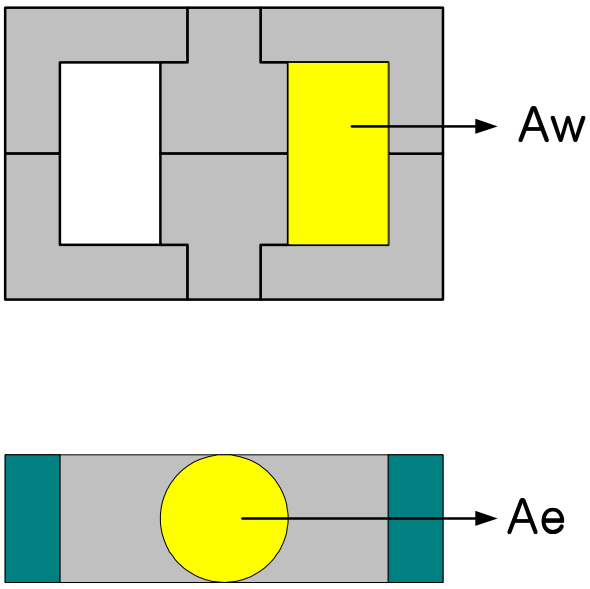


Figure 6. Window Area and Cross Sectional Area

With a determined core, the minimum number of turns for the transformer primary side to avoid saturation is given by

$$N_p^{min} = \frac{V_{DC}^{min} \cdot D_{max}}{A_e \cdot f_s \cdot \Delta B} \times 10^6 \quad (turns) \quad (14)$$

(6) STEP-6 : Determine the number of turns for each inding of the transformer

First, determine the turns ratio between the primary side and the feedback controlled secondary side as a reference.

$$n = \frac{N_p}{N_{sl}} = \frac{V_{DC}^{min} \cdot D_{max}}{V_{o1} + V_{F1}} \quad (15)$$

where N_p and N_{s1} are the number of turns for primary side and reference output, respectively. V_{o1} is the output voltage and V_{F1} is the diode forward voltage drop of the reference output.

Then, determine the proper integer numbers for N_{s1} so that the resulting N_p is larger than Npmin obtained from equation (14). The magnetizing inductance of the primary side is given by

$$L_m = A_L \times N_p^2 \times 10^{-9} \quad (H) \quad (16)$$

where A_L is the AL-value with no gap in nH/turns^2.

The numer of turns for the n-th output is determined as

$$N_{S(n)} = \frac{V_{o(n)} + V_{F(n)}}{V_{o1} + V_{F1}} \cdot N_{s1} \quad (turns) \quad (17)$$

where $V_{o(n)}$ is the output voltage and $V_{F(n)}$ is the diode forward voltage drop of the n-th output.

The next step is to determine the number of turns for Vcc winding. The number of turns for Vcc winding is determined differently according to the reset method.

(a) <u>Auxiliary winding reset</u> : For auxiliary winding reset, the number of turns of the Vcc winding is obtained as

$$N_a = \frac{V_{cc}^* + V_{Fa}}{V_{DC}^{min}} \cdot N_r \quad (turns) \quad (18)$$

where Vcc* is the nominal voltage for Vcc and V_{Fa} is the diode forward voltage drop. Since Vcc is proportional to the input voltage when auxiliary winding reset is used, it is proper to set Vcc* as the Vcc start voltage to avoid the over voltage protection during the normal operation.

(b) <u>RCD reset</u> : For RCD reset, the number of turns of the Vcc winding is obtained as

$$N_a = \frac{V_{cc}^* + V_{Fa}}{V_{sn}} \cdot N_p \quad (turns) \quad (19)$$

where Vcc* is the nominal voltage for Vcc. Since Vcc is almost constant for RCD reset in normal operation, it is proper to set Vcc* to be 2-3 V higher than Vcc start voltage.

(7) STEP-7 : Determine the wire diameter for each transformer winding based on the rms current.

The rms current of the n-th winding is obtained as

$$I_{sec(n)}^{rms} = I_{o(n)} \sqrt{(3 + K_{RF}^2)\frac{D_{max}}{3}} \quad (20)$$

where $I_{o(n)}$ is the maximum current of n-th output.

When the auxiliary winding reset is employed, the rms current of the reset winding is as follows.

$$I_{Reset}^{rms} = \frac{V_{DC}^{min} D_{max}}{L_m f_s}\sqrt{\frac{D_{max}}{3}} \qquad (21)$$

The current density is typically 5A/mm^2 when the wire is long (>1m). When the wire is short with small number of turns, current density of 6-10 A/mm^2 is also acceptable. Avoid using wire with a diameter larger than 1 mm to avoid severe eddy current losses and to make winding easier. For high current output, it is better to use parallel winding with multiple strands of thinner wire to minimize skin effect.

Check if the winding window area of the core is enough to accommodate the wires. The required window area is given by

$$A_w = A_c / K_F \qquad (22)$$

where A_c is the actual conductor area and K_F is the fill factor. Typically the fill factor is 0.2-0.3 when a bobbin is used.

(8) STEP-8 : Determine the proper core and the number of turns for output inductor

When the forward converter has more than one output as shown in figure 7, coupled inductors are usually employed to improve the cross regulation, which are implemented by winding their separate coils on a single, common core.

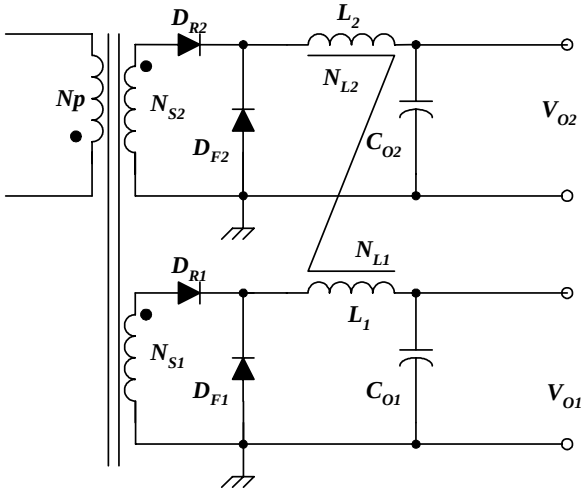


Figure 7. Coupled Output Inductors

First, determine the turns ratio of the n-th winding to the reference winding (the first winding) of the coupled inductor. The turns ratio should be the same with the transformer turns ratio of the two outputs as follows.

$$\frac{N_{S(n)}}{N_{S1}} = \frac{N_{L(n)}}{N_{L1}} \qquad (23)$$

Then, calculate the inductance of the reference output inductor as

$$L_1 = \frac{V_{o1}(V_{o1} + V_{F1})}{2 \cdot f_s \cdot K_{RF} \cdot P_o}(1 - D_{min}) \qquad (24)$$

$$\text{where} \qquad D_{min} = D_{max} \cdot \frac{V_{DC}^{min}}{V_{DC}^{max}} \qquad (25)$$

The minimum number of turns for L_1 to avoid saturation is given by

$$N_{L1}^{min} = \frac{L_1 P_O (1 + K_{RF})}{V_{O1} B_{sat} A_e} \times 10^6 \quad (turns) \qquad (26)$$

where I_{lim} is the FPS current limit level, A_e is the cross sectional area of the core in mm^2 and B_{sat} is the saturation flux density in tesla. If there is no reference data, use B_{sat} =0.35-0.4 T. Once N_{L1} is determined, $N_{L(n)}$ is determined by equation (23).

(9) STEP-9 : Determine the wire diameter for each inductor winding based on the rms current.

The rms current of the n-th inductor winding is obtained as

$$I_{L(n)}^{rms} = I_{o(n)}\sqrt{\frac{(3 + K_{RF}^2)}{3}} \qquad (27)$$

The current density is typically 5A/mm^2 when the wire is long (>1m). When the wire is short with small number of turns, a current density of 6-10 A/mm^2 is also acceptable. Avoid using wire with diameter larger than 1 mm to avoid severe eddy current losses and to make winding easier. For high current output, it is better to use parallel winding with multiple strands of thinner wire to minimize skin effect.

(10) STEP-10 : Determine the diode in the secondary side based on the voltage and current ratings.

The maximum voltage and the rms current of the rectifier diode of the n-th output are obtained as

$$V_{D(n)} = V_{DC}^{max} \frac{N_{S(n)}}{N_P} \qquad (28)$$

$$I_{D(n)}^{rms} = I_{o(n)}\sqrt{(3 + K_{RF}^2)\frac{D_{max}}{3}} \qquad (29)$$

(11) STEP-11 : Determine the output capacitor considering the voltage and current ripple.

The ripple current of the n-th output capacitor is obtained as

$$I_{C(n)}^{rms} = \frac{K_{RF} I_{o(n)}}{\sqrt{3}} \quad (30)$$

The ripple current should be equal to or smaller than the ripple current specification of the capacitor.

The voltage ripple on the n-th output is given by

$$\Delta V_{o(n)} = \frac{I_{o(n)} \cdot K_{RF}}{4 C_{o(n)} f_s} + 2 K_{RF} I_{o(n)} R_{c(n)} \quad (31)$$

where $C_{o(n)}$ is the capacitance and $R_{c(n)}$ is the effective series resistance (ESR) of the n-th output capacitor.

Sometimes it is impossible to meet the ripple specification with a single output capacitor due to the high ESR of the electrolytic capacitor. Then, additional LC filter (post filter) can be used. When using additional LC filter, be careful not to place the corner frequency too low. If the corner frequency is too low, it may make the system unstable or limit the control bandwidth. It is proper to set the corner frequency of the filter to be around 1/10 to 1/5 of the switching frequency.

(12) STEP-12 : Design the Reset circuit.

(a) <u>Auxiliary winding reset</u> : For auxiliary winding reset, the maximum voltage and rms current of the reset diode are given by

$$V_{Dreset} = V_{DC}^{max}\left(1 + \frac{N_r}{N_p}\right) \quad (32)$$

$$I_{Dreset}^{rms} = \frac{V_{DC}^{min} D_{max}}{L_m f_s}\sqrt{\frac{D_{max}}{3}} \quad (33)$$

(b) <u>RCD reset</u> : For RCD reset, the maximum voltage and rms current of the reset diode are given by

$$V_{DR} = V_{DC}^{max} + V_{sn} \quad (34)$$

$$I_{DR}^{rms} = \frac{V_{DC}^{min} D_{max}}{L_m f_s}\sqrt{\frac{D_{max}}{3}} \quad (35)$$

The power loss of the snubber network in normal operation is obtained as

$$Loss_{sn} = \frac{V_{sn}^2}{R_{sn}} = \frac{1}{2}\left[\frac{(nV_{o1})^2}{L_m f_s} - \frac{2nV_{o1}V_{sn}}{\sqrt{L_m / C_{oss}}}\right] \quad (36)$$

where V_{sn} is the snubber capacitor voltage in normal operation, R_{sn} is the snubber resistor, n is N_p/N_{s1} and C_{oss} is the ouput capacitance of the MOSFET. Based on the power loss, the snubber resistor with proper rated wattage should be chosen.

The ripple of the snubber capacitor voltage in normal operation is obtained as

$$\Delta V_{sn} = \frac{V_{sn} D_{max}}{C_{sn} R_{sn} f_s} \quad (37)$$

In general, 5-10% ripple is practically reasonable.

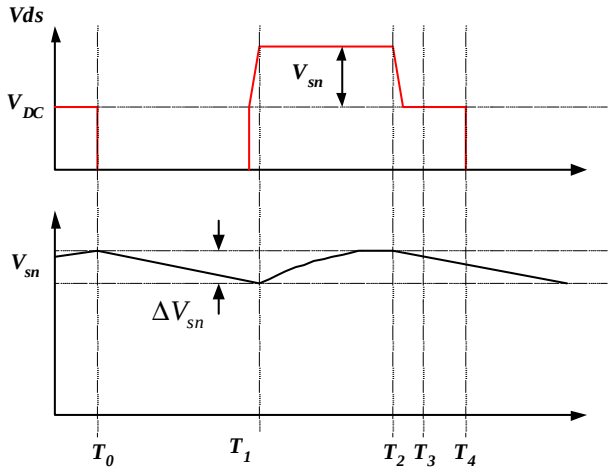


Figure 8. Snubber Capacitor Voltage

(13) STEP-13 : Design the feed back loop.

Since FPS employs current mode control as shown in figure 9, the feedback loop can be simply implemented with a one pole and one zero compensation circuit.

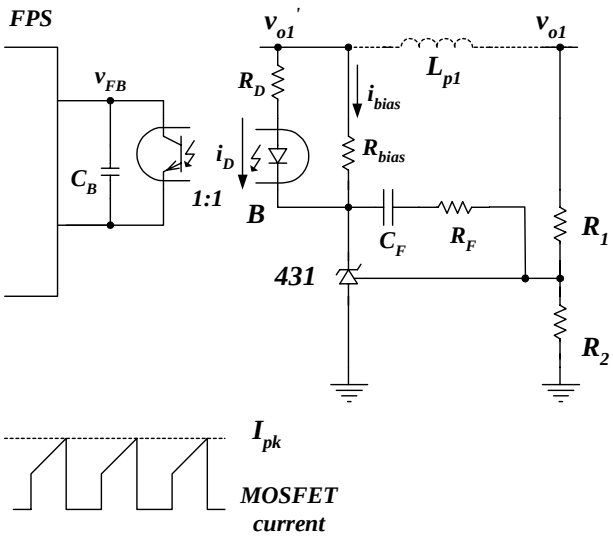


Figure 9. Control Block Diagram

For continuous conduction mode (CCM) operation, the control-to-output transfer function of forward converter using FPS is given by

$$G_{vc} = \frac{\hat{v}_{o1}}{\hat{v}_{FB}} = K \cdot R_L \cdot \frac{N_p}{N_{s1}} \cdot \frac{1 + s/w_z}{1 + s/w_p} \qquad (38)$$

$$\text{where} \quad w_z = \frac{1}{R_{c1}C_{o1}}, \qquad w_p = \frac{1}{R_L C_{o1}}$$

and R_L is the effective total load resistance of the controlled output defined as V_{o1}^2/P_o.When the converter has more than one output, the DC and low frequency control-to-output transfer function are proportional to the parallel combination of all load resistance, adjusted by the square of the turns ratio. Therefore, the effective total load resistance is used in equation (38) instead of the actual load resistance of V_{o1}.

The voltage-to-current conversion ratio of FPS, K is defined as

$$K = \frac{I_{pk}}{V_{FB}} = \frac{I_{lim}}{3} \qquad (39)$$

where I_{pk} is the peak drain current and V_{FB} is the feedback voltage for a given operating condition.
Figure 10 shows the variation of control-to-output transfer function for a CCM forward converter according to the load. Since a CCM forward converter has inherent good line regulation, the transfer function is independent of input voltage variation. While the system pole together with the DC gain changes according to the load condition.

The feedback compensation network transfer function of figure 9 is obtained as

$$\frac{\hat{v}_{FB}}{\hat{v}_{o1}} = -\frac{w_i}{s} \cdot \frac{1 + s/w_{zc}}{1 + 1/w_{pc}} \qquad (40)$$

$$\text{where } w_i = \frac{R_B}{R_1 R_D C_F s}, w_{zc} = \frac{1}{(R_F + R_1)C_F}, w_{pc} = \frac{1}{R_B C_B}$$

As can be seen in figure 10, the worst case in designing the feedback loop for a CCM forward converter is the full load condition. Therefore, by designing the feedback loop with proper phase and gain margin in low line and full load condition, the stability all over the operation ranges can be guaranteed.

The procedure to design the feedback loop is as follows:

(a) Determine the crossover frequency (f_c). When an additional LC filter (post filter) is employed, the crossover frequency should be placed below 1/3 of the corner frequency of the post filter, since it introduces -180 degrees phase drop. Never place the crossover frequency beyond the corner frequency of the post filter. If the crossover frequency is too close to the corner frequency, the controller should be designed to have enough phase margin more than about 90 degrees when ignoring the effect of the post filter.

(b) Determine the DC gain of the compensator (w_i/w_{zc}) to cancel the control-to-output gain at f_c.

(c) Place compensator zero (f_{zc}) around $f_c/3$.
(d) Place compensator pole (f_{pc}) above $3f_c$.

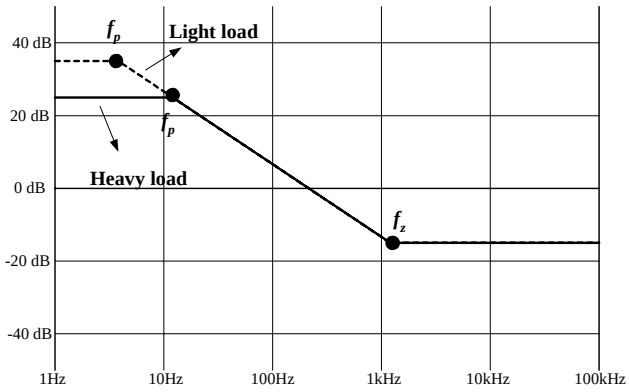


Figure 10. CCM Forward Converter Control-to-output Transfer Function variation According to the Load

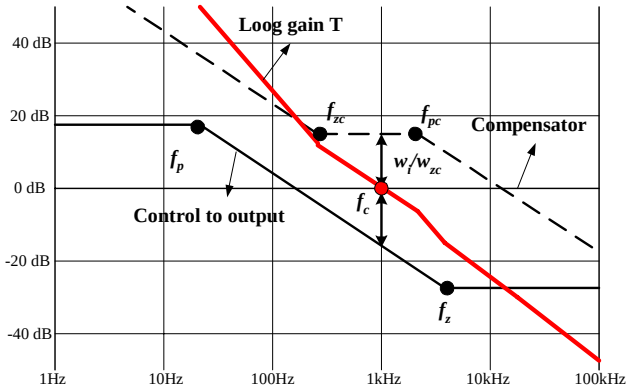


Figure 11. Compensator Design

When determining the feedback circuit component, there are some restrictions as follows.

(a) The capacitor connected to feedback pin (C_B) is related to the shutdown delay time in an overload situation as

$$T_{delay} = (V_{SD} - 3) \cdot C_B / I_{delay} \qquad (41)$$

where V_{SD} is the shutdown feedback voltage and I_{delay} is the shutdown delay current. These values are given in the data sheet. In general, 10~100 ms delay time is proper for most practical applications. In some cases, the bandwidth may be limited due to the required delay time in over load protection.

(b) The resistor R_{bias} and R_D used together with opto-coupler and the KA431 should be designed to provide proper operating current for the KA431 and to guarantee the full swing of the feedback voltage of the FPS. In general, the minimum cathode voltage and current for KA431 is 2.5V and 1mA, respectively. Therefore, R_{bias} and R_D should be designed to satisfy the following conditions.

$$\frac{V_o - V_{OP} - 2.5}{R_D} > I_{FB} \quad (42)$$

$$\frac{V_{OP}}{R_{bias}} > 1mA \quad (43)$$

where V_{OP} is opto-diode forward voltage drop, which is typically 1V and I_{FB} is the feedback current of FPS, which is typically 1mA. For example, R_{bias}<1kΩ and R_D <1.5kΩ for V_{o1}=5V.

- Summary of symbols -

A_w : Window area of the core in mm^2
Ae : Cross sectional area of the core in mm^2
B_{sat} : Saturation flux density in tesla.
ΔB : Maximum flux density swing in tesla in normal operation
C_o : Capacitance of the output capacitor.
D_{max} : Maximum duty cycle ratio
E_{ff} : Estimated efficiency
f_L : Line frequency
f_s : Switching frequency
I_{ds}^{peak} : Maximum peak current of MOSFET
I_{ds}^{rms} : RMS current of MOSFET
I_{lim} : FPS current limit level.
$I_{sec(n)}^{rms}$: RMS current of the n-th secondary winding
$I_{D(n)}^{rms}$: Maximum rms current of the rectifier diode for the n-th output
$I_{c(n)}^{rms}$: RMS Ripple current of the n-th output capacitor
I_O : Output load current
$K_{L(n)}$: Load occupying factor for n-th output
K_{RF} : Current ripple factor
L_m : Transformer primary side inductance
$Loss_{sn}$: Power loss of the snubber network in normal operation
N_p^{min} : The minimum number of turns for the transformer primary side to avoid saturation
N_p : Number of turns for primary side
N_r : Number of turns for reset winding
N_{s1} : Number of turns for the reference output
P_o : Maximum output power
P_{in} : Maximum input power
R_c : Effective series resistance (ESR) of the output capacitor.
R_{sn} : Snubber resistor
R_L : Output load resistor
V_{line}^{min} : Minimum line voltage
V_{line}^{max} : Maximum line voltage
V_{DC}^{min} : Minimum DC link voltage
V_{DC}^{max} : Maximum DC line voltage
V_{ds}^{nom} : Maximum nominal MOSFET voltage
V_{o1} : Output voltage of the reference output.
V_{F1*} : Diode forward voltage drop of the reference output.
V_{cc*} : Nominal voltage for Vcc
V_{Fa} : Diode forward voltage drop of Vcc winding
ΔV_{DC}^{max} : Maximum DC link voltage ripple
$V_{D(n)}$: Maximum voltage of the rectifier diode for the n-th output
$\Delta V_{o(n)}$: Output voltage ripple of the n-th output
V_{sn} : Snubber capacitor voltage in normal operation
ΔV_{sn} : Snubber capacitor voltage ripple
V_{sn}^{max} : Maximum snubber capacitor voltage during transient or over load situation
V_{ds}^{max} : Maximum voltage stress of MOSFET

Appendix. Design Example using FPS design Assistant

Target System : PC Power Supply

- Input : universal input (90V-265Vrms) with voltage doubler
- Output : 5V/15A, 3.3V/10A, 12V/6A

FAIRCHILD SEMICONDUCTOR™

FPS Design Assistant ver.1.0 By Choi
For forward converter with reset winding

Blue cell is the input parameters
Red cell is the output parameters

1. Define specifications of the SMPS

Minimum Line voltage (V_line.min)	180	V.rms
Maximum Line voltage (V_line.max)	265	V.rms
Line frequency (fL)	60	Hz

	Vo		Io		Po		KL	
1st output for feedback	5	V	15	A	75	W	42	%
2nd output	3.3	V	10	A	33	W	18	%
3rd output	12	V	6	A	72	W	40	%
4th output	0	V	0	A	0	W	0	%
Maximum output power (Po) =	180.0	W						
Estimated efficiency (Eff)	70	%						
Maximum input power (Pin) =	257.1	W						

2. Determine DC link capacitor and the DC voltage range

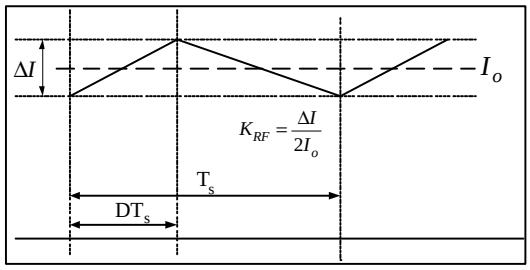
DC link capacitor	235	uF
DC link voltage ripple =	29	V
Minimum DC link voltage =	226	V
Maximum DC link voltage =	375	V

3. Determine the maximum duty ratio (Dmax)

Maximum duty ratio	0.4		
Turns ratio (Np/Nr)	1	>	0.67
Maximum nominal MOSFET voltage =	750	V	

4. Determine the ripple factor of the output inductor current

Output Inductor current ripple factor	0.15	
Maximum peak drain current =	3.27	A
RMS drain current =	1.81	A
Current limit of FPS	4	A



5. Determine proper core and minimum primary turns for transformer

Switching frequency of FPS (kHz)	67	kHz	
Maximum flux density swing	0.32	T	--> EER2834
Estimated AP value of core =	9275	mm^4	AP=12470
Cross sectional area of core (Ae)	86	mm^2	Ae=86
Minimum primary turns =	49.0	T	Aw=145

6. Determine the numner of turns for each outputs

	Vo		VF			# of turns	
Vcc (Use Vcc start voltage)	15	V	1.2	V	3.6 =>	4	T
1st output for feedback	5	V	0.4	V	3 =>	3	T
2nd output	3.3	V	0.4	V	2.06 =>	2	T
3rd output	12	V	0.5	V	6.94 =>	7	T
4th output	0	V	0	V	0 =>	0	T
VF : Forward voltage drop of rectifier diode					Reset winding =	50	T
					Primary turns =	50	T
					->enough turns		
AL value (no gap)	2490	nH/T^2					
Transformer magnetizing inductance =	6.27499	mH			--> EER2834		

7. Determine the wire diameter for each transformer winding

	Diameter		Parallel		Irms		(A/mm^2)
Primary winding (Np)	0.68	mm	1	T	1.81	A	4.98
Reset winding (Nr)	0.31	mm	1	T	0.08	A	1.04
Vcc winding	0.31	mm	1	T	0.10	A	1.33
1st output winding	0.68	mm	4	T	9.5	A	6.56
2nd output winding	0.68	mm	3	T	6.3	A	5.83
3rd output winding	0.68	mm	2	T	3.8	A	5.25
4th output winding	0	mm	0	T	0.0	A	#DIV/0!
Copper area =	33.9262	mm^2					
Fill factor	0.25						
Required window area	135.705	mm^2	--> EER2834 (Aw=145)				

8. Determine proper core and number of turns for inductor (coupled inductor)

Cross sectional area of Inductor core (A	86	mm^2	--> EER2834	
Saturation flux density	0.42	T		
Inductance of 1st output (L1) =	5.7	uH		
Minimum turns of L1 =	6.5	T		
Actual number of turns for L1	6	=>	6	T
Number of turns for L2 =	4	=>	4	T
Number of turns for L3 =	14	=>	14	T
Number of turns for L4 =	0	=>	0	T

9. Determine the wire diameter for each inductor winding

	Diameter		Parallel		Irms		(A/mm^2)
Winding for L1	0.68	mm	5	T	15.1	A	8.30
Winding for L2	0.68	mm	3	T	10.0	A	9.22
Winding for L3	0.68	mm	2	T	6.0	A	8.30
Winding for L4	0	mm	0	T	0.0	A	#DIV/0!
Copper area =	25.4089	mm^2					
Fill factor	0.25						
Required window area	101.636	mm^2	--> EER2834(Aw=145)				

10. Determine the rectifier diodes in the secondary side

	Reverse voltage		Rms Current		
Vcc diode	55	V	0.10	A	-->UF4003
1st output diode	22	V	9.5	A	-->MBR3060PT
2nd output diode	15	V	6.3	A	-->MBR3045PT
3rd output diode	52	V	3.81	A	-->MBR20H100CT
4th output diode	0	V	0.00	A	

11. Determine the output capacitor

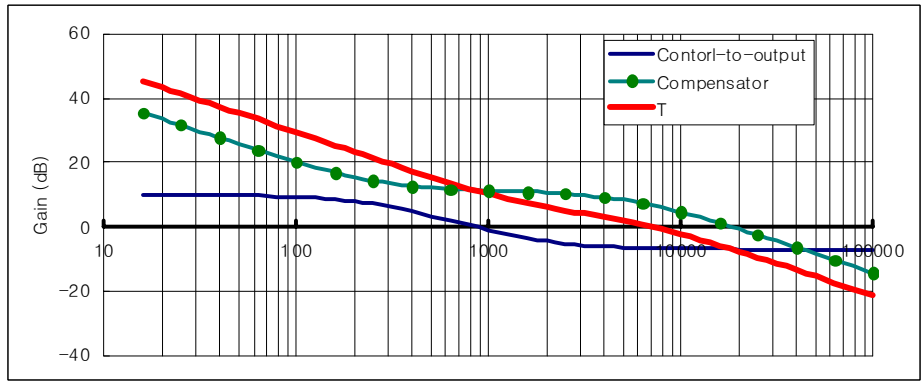
	Capacitance		ESR		Current ripple		Voltage Ripple	
1st output capacitor	4400	uF	20	mΩ	1.3	V	0.09	V
2nd output capacitor	4400	uF	20	mΩ	0.9	V	0.06	V
3rd output capacitor	2000	uF	60	mΩ	0.5	V	0.11	V
4th output capacitor	0	uF	0	mΩ	0.0	V	####	V

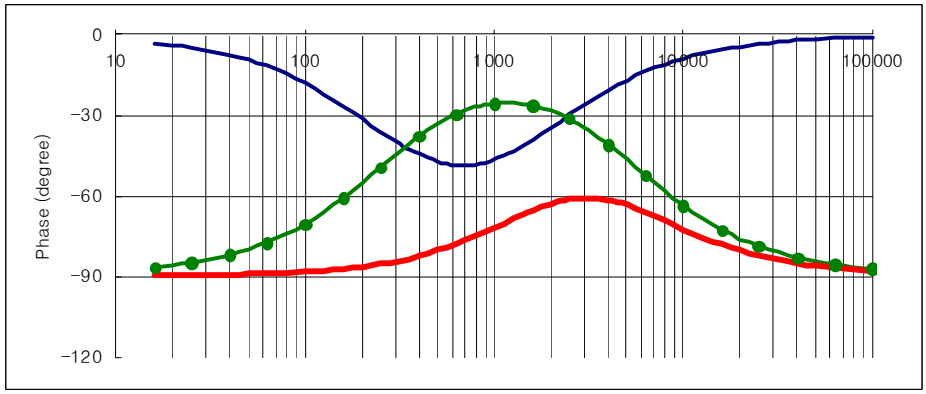
12. Design the Reset Circuit

Reset diode rms current	0.08	A	
Maximum voltage of reset diode	750	V	-->UF4007

13. Design Feedback control loop

Control-to-output DC gain =	3	
Control-to-output zero =	1,809	Hz
Control-to-output pole =	261	Hz
Voltage divider resistor (R1)	5	kΩ
Voltage divider resistor (R2)	5	kΩ
Opto coupler diode resistor (RD)	1	kΩ
431 Bias resistor (Rbias)	1.2	kΩ
Feeback pin capacitor (CB) =	10	nF
Feedback Capacitor (CF) =	100	nF
Feedback resistor (RF) =	1	kΩ
Feedback integrator gain (fi) =	955	Hz
Feedback zero (fz) =	265.393	Hz
Feedback pole (fp) =	5307.86	Hz





Design Summary

- For the FPS, FS7M0880 is chosen. This device has a fixed switching frequency of 67kHz.
- To limit the current, a 10 ohm resistor (Ra) is used in series with the Vcc diode.
- The control bandwidth is 6kHz. Since the crossover frequency is too close the corner frequency of the post filter (additional LC filter), the controller is designed to have enough phase margin of 120 degrees when ignoring the effect of the post filter.

Figure 12 shows the final schematic of the forward converter designed by *FPS Design Assistant*

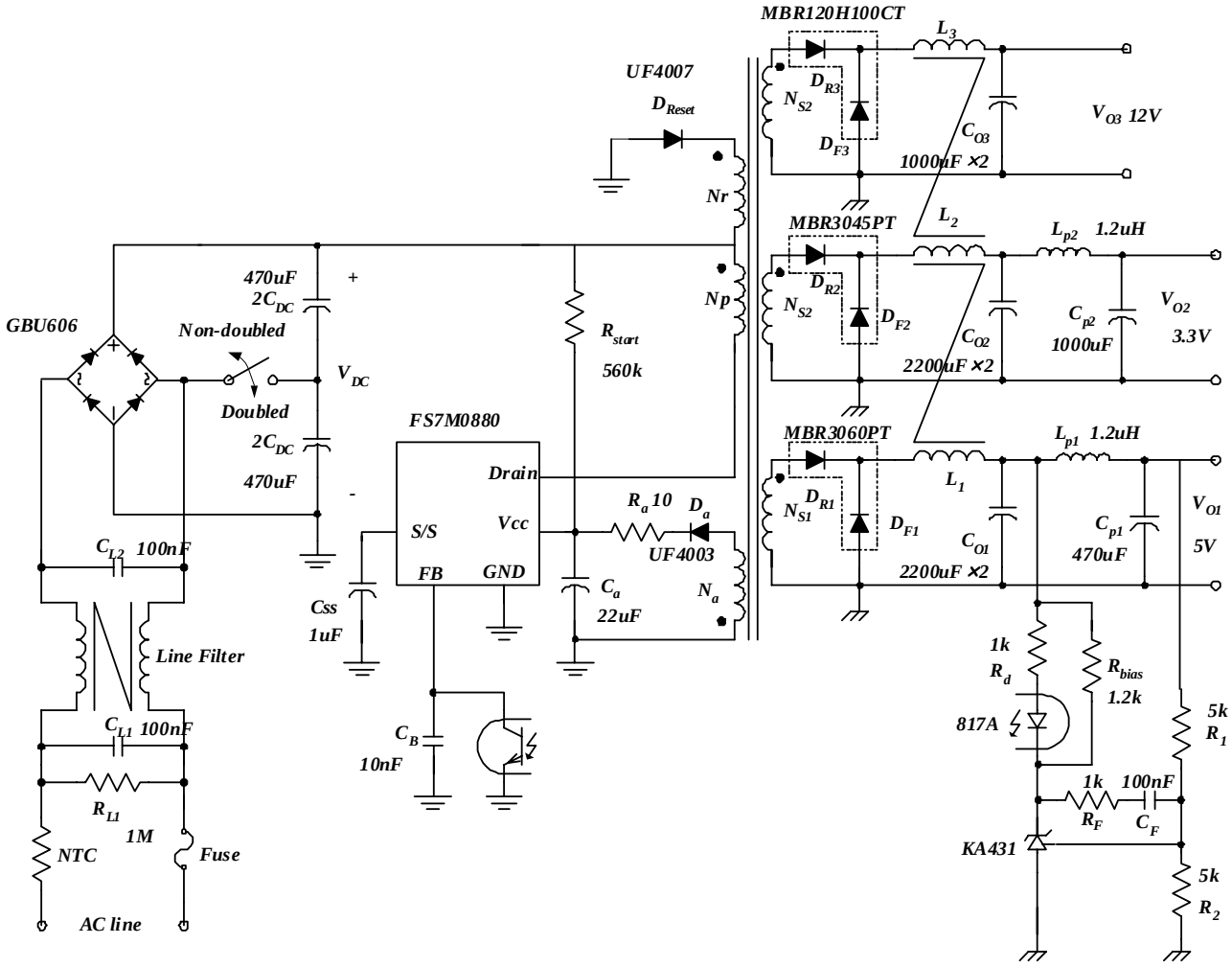


Figure 12. The final schematic of the forward converter

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Application Note AN-4105

Design Considerations for Switched-Mode Power Supplies Using a Fairchild Power Switch (FPS) in a Flyback Converter

Introduction

Flyback, switched-mode power supplies (SMPS) are among the most frequently used power circuits in household and consumer electronics. The basic function of an SMPS is to supply regulated power to the load on the secondary, or output, side. An SMPS typically incorporates a power transformer, secondary-side rectifier diodes, a switching semiconductor device with control IC, and peripheral circuitry. If the level of integration of the switching and control circuitry is not high enough, then additional, separate circuits are required to accommodate all functions. Such additional components raise the overall SMPS cost and sometimes reduce reliability.

Fairchild power switches are highly integrated ICs for power supply applications. They combine a high-voltage power MOSFET (SenseFET) and pulse width modulation (PWM)-based control IC in one package. Moreover, they provide enhanced IC functionality, thereby minimizing the number of additional components needed in an SMPS. Fairchild Power Switch (FPS) ICs are widely used in the power circuits of a variety of equipment, such as color TVs, printers, PCs, monitors, battery chargers, and AC adapters. They typically incorporate a variety of enhanced protection functions and they greatly reduce power consumption in standby modes.

This application note considers the three major functional blocks of an SMPS: Fairchild Power Switch (FPS), flyback converter, and transformer. It discusses a variety of issues important to their design and use in the overall SMPS.

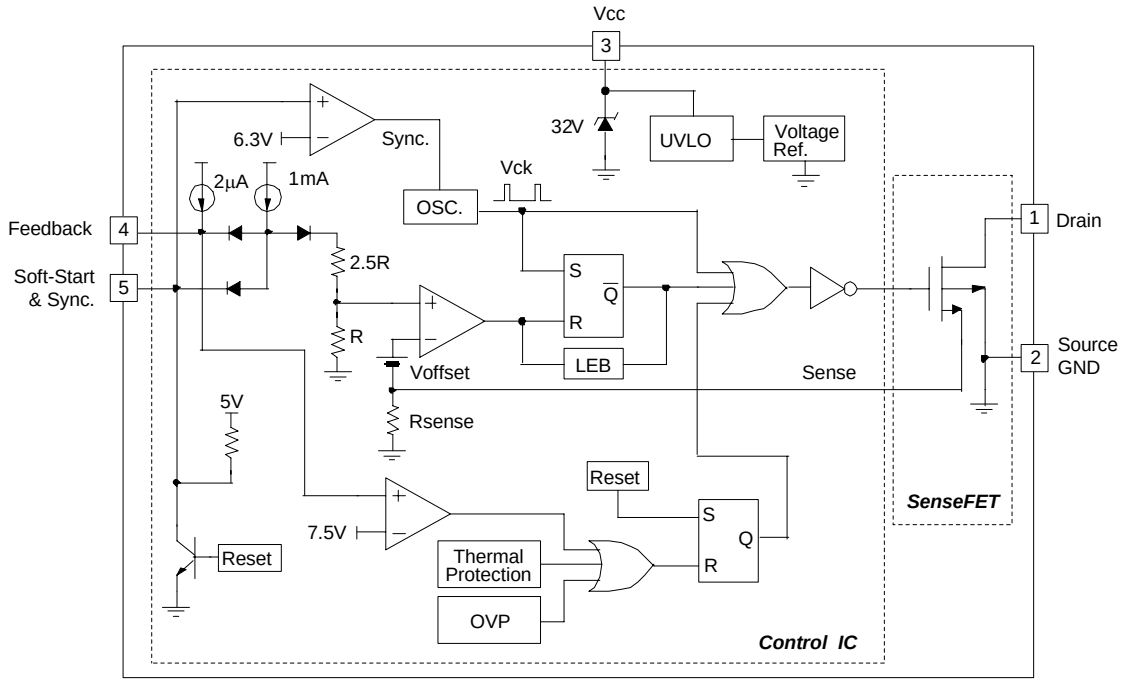


Figure1. Internal block diagram of a Fairchild Power Switch (FPS)

1. Block Diagram and Basic Operation of a Fairchild Power Switch (FPS)

1.1 Block Diagram

Figure 1 presents a block diagram of a Fairchild Power Switch (FPS). It can be divided into several large, functional sections: under-voltage lockout circuitry (UVLO); reference voltage; oscillator (OSC); pulse width modulation (PWM) block; protection circuits; and gate driving circuits.

1.2 Under-Voltage Lockout (UVLO)

A Fairchild Power Switch (FPS) under-voltage lockout (UVLO) circuitry (Figure 2) guarantees stable operation of the IC's control circuit by stopping and starting it as a function of the value of V_{CC} (Figure 3). The turn off and turn on voltage thresholds are fixed internally at 10V and 15V, respectively; therefore, the UVLO circuitry turns off the control circuit when V_{CC} is lower than 10V and starts it when V_{CC} is higher than 15V. Once the control circuit starts operating, V_{CC} must drop below the 10V level for the UVLO to stop the circuit again. Before switching starts, the IC current is less than 300µA. IC operation starts when C_{CC} (Figure 2) charges to 15V. Because only a small current (<1mA) is allowed to flow in through the resistor during normal operation, this technique reduces the current dissipation in the SMPS start-up resistor.

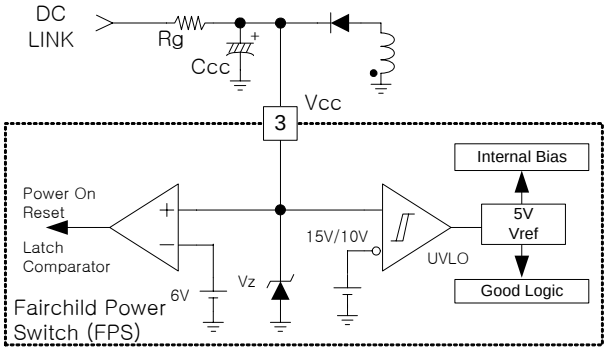


Figure 2. Detail of the under-voltage lockout (UVLO) circuitry in a Fairchild Power Switch. The gate operating circuit holds in a low state during UVLO, thereby maintaining the SenseFET at turn-off

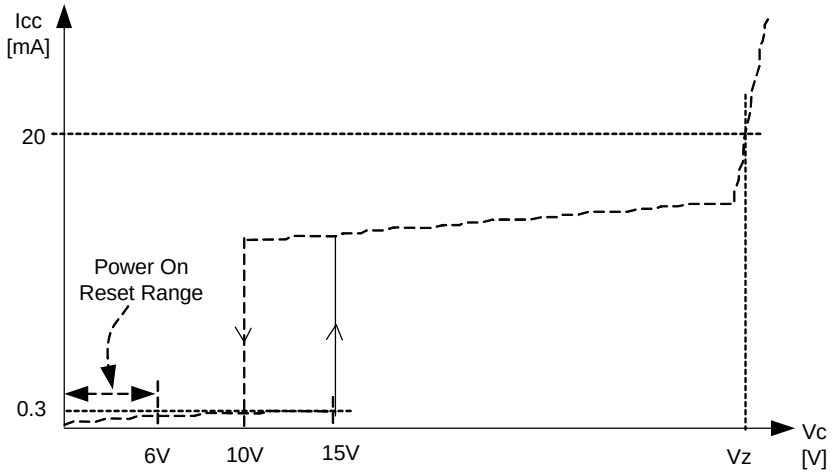


Figure 3. Fairchild Power Switch (FPS) control circuit status vs. V_{cc}

1.3 Feedback Control Circuit

The Fairchild Power Switch (FPS) control IC uses a current mode PWM and operates such that MOSFET current is proportional to the feedback voltage V_{fb}. This limits the MOSFET current at every cycle. It also offers other advantages, such as a well-regulated SMPS output voltage with input voltage changes. This method of control also works successfully in SMPSs used for monitors, which may have a broad range of synchronizing frequencies to accommodate. As shown in Figure 4, the Fairchild Power Switch (FPS) oscillator turns on the MOSFET. The feedback comparator operates to turn it off again when the MOSFET current reaches a set value proportional to V_{fb}. The MOSFET turn-off operation is as follows: (1) the internal (R+2.5R) voltage divider sets the voltage fed back to one input of the feedback comparator at V_{fb} /3.5; (2) a current proportional to the drain current flows to the MOSFET sense terminal, making V_{sense} proportional to the drain current; and, (3) when V_{sense} becomes greater than V_{fb}, the output of the feedback comparator goes high, turning off the MOSFET. Figure 4 also shows that the circuit is designed to

use an opto isolator in the feedback loop. This is appropriate for an off-line design where input to output isolation is required. C_{fb} improves the noise characteristics. If the control IC incorporates an error amp as in Fairchild's KA3842B/3B/4B/5B current mode PWM controller ICs for SMPSs, a resistor and capacitor are required to provide the feedback to the error amp. This would provide the same functions as those provided by the circuit of Figure 4; fine control of the output voltage through Vfb. Similarly, other appropriate devices are Fairchild's LM431/TL431/KA431 series of three terminal shunt regulators. These have a very sharp turn-on characteristic much like a Zener diode and are widely used in SMPS secondary-side error amplifiers.

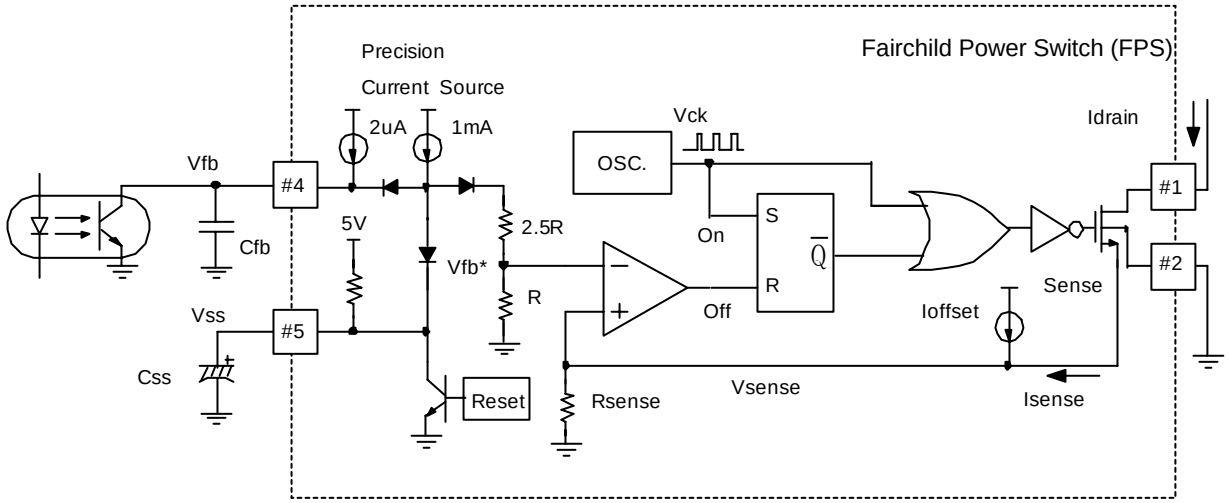
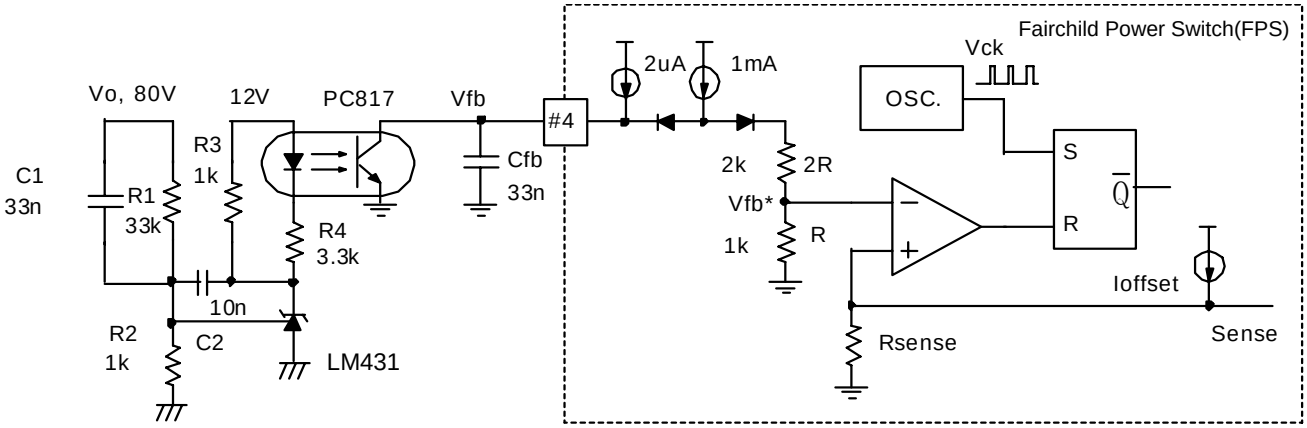


Figure 4. Fairchild Power Switch (FPS) feedback circuit appropriate for off-line SMPS use (current mode PWM)

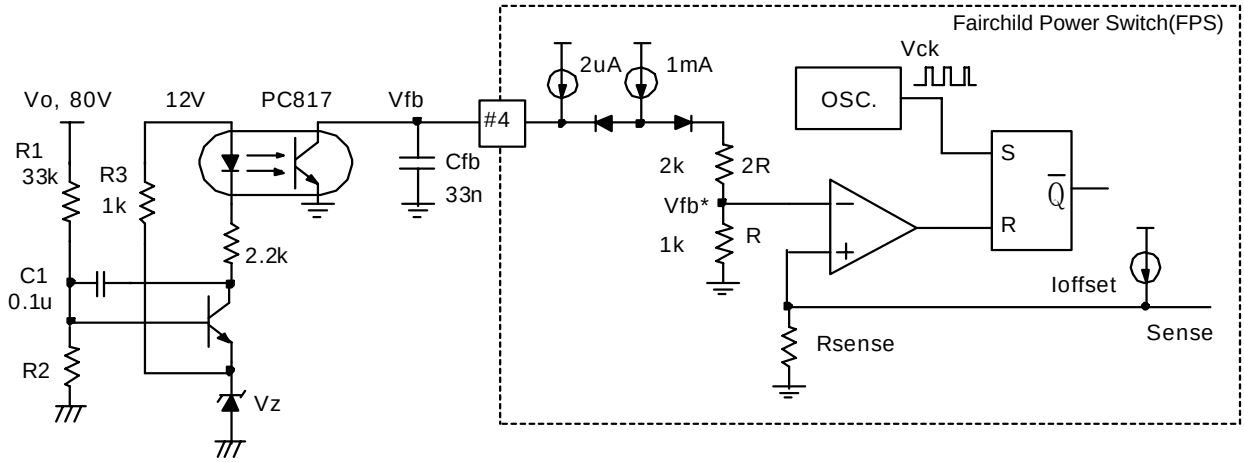
1.4 Example Fairchild Power Switch (FPS) Control Circuit

Figure 5 shows two approaches to control feedback with a Fairchild Power Switch (FPS). The design in Figure 5a uses the LM431 regulator and that of Figure 5b uses a Zener diode. Even though the Zener diode approach is cost effective, the output regulation is relatively poor.

In Figure 5a, C1, together with R1, produces a high-frequency pole formed by the internal 3.5kΩ resistor and C_{fb} in the compensation network. R4 limits the maximum current of the photodiode to 2.3mA [(12V - 2.5V - 2V) /3.3KΩ, where 2.5V is the LM431's saturation voltage and 2 V is the photodiode's voltage drop]. C_{fb} should be determined by considering the shutdown delay time (see Section 2.1). In Figure 5b, R3 sets a fixed current to the Zener diode to stabilize its voltage.



(a) Control Circuit using KA431(LM431) Control IC



(b) Control Circuit using a Zener Diode Control IC

Figure 5. Fairchild Power Switch (FPS) feedback control circuit

1.5 Soft-Start Operation

Normally, the SMPS output voltage increases from start up with a fixed time constant. This is due to the capacitive component of the load. At start up, therefore, the feedback signal applied to the PWM comparator's inverting input reaches its maximum value (1V) because the feedback loop is effectively open. Also at this time, the drain current is at its peak value (I_{peak}) and maximum allowable power is being delivered to the secondary load. When the SMPS pushes maximum power to the secondary side for this initial fixed time, the entire circuit is seriously stressed. Use of a soft-start function avoids such stresses. Figure 6 shows how to implement a soft-start for a Fairchild Power Switch (FPS). At turn on, the soft-start capacitor C_S on pin 5 of the Fairchild Power Switch (FPS) starts to charge through the 1mA current source. When the voltage across C_S reaches 3V, diode D_S turns off. No more current flows to it from the 1mA current source. Cs then continues to charge to 5V through the 50kΩ resistor.

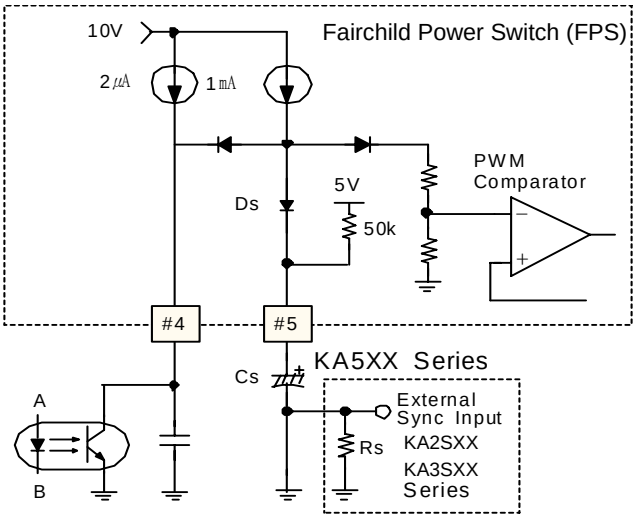


Figure 6. Soft-start circuit

When the voltage across C_S exceeds 3V, the voltage at the comparator's inverting terminal no longer follows the voltage across C_S. Instead, it follows the output voltage feedback signal. In shutdown or protection circuit operation, capacitor C_S is discharged, to enable it to charge from 0V at restart.

1.6 Synchronization

In an SMPS intended for use with monitors, synchronization is handled differently from a general purpose SMPS. For monitor use, it is necessary to prevent noise from appearing on the monitor display. To accomplish this, it is necessary to synchronize the SMPS switching frequency with the monitor's horizontal sync frequency. The monitor's horizontal scan flyback signal is commonly used as the external sync signal for the SMPS. By synchronizing the switching with the horizontal scan's flyback, the switching noise is positioned at the far left of the monitor display where it cannot be seen.

Figure 7 shows how to implement the external circuit for synchronization. The external sync signal, applied across resistor R_s, cannot drop below 0.6V because of diode D_{sync}. After the conclusion of the initial soft start, the voltage across C_s remains at 5V until the external sync signal is applied, at which point, it looks like V_{Rs} of Figure 8. The sync comparator compares V_{Cs} against a 6.3V level and produces the comparator output waveform, V_{comp} of Figure 8.

A Fairchild Power Switch (FPS) has an internal timing capacitor, C_t. Figure 8 shows that when the voltage on C_t, V_{Ct}, reaches an upper threshold, it begins to discharge; then, when it reaches a lower threshold, it again starts to charge. This operation is controlled by the internal oscillator. The oscillator output signal, V_{Ck} in Figure 8, which goes low when C_t recharges and high when it discharges, is applied to the Fairchild Power Switch (FPS) S/R Latch Set terminal. In the absence of an external sync signal, the voltage across C_t oscillates at the basic frequency of 20kHz. In the presence of a sync signal, however, the Set signal goes high because V_{Ct} charges to the high threshold following the external sync signal and, ultimately, the Set signal, which determines the switching frequency, synchronizes to the external sync signal. It is necessary to limit the Set signal's high duration to 5% or less of the full cycle. As the Set signal drops low, the gate turns on. If the device is not synchronized to the horizontal scan of the monitor, noise appears on the screen. When the Set signal goes high, the sync is synchronized with the horizontal scan flyback. Because the high duration is 5% (maximum) of the full cycle, the start of the horizontal scan (as the Set signal goes low) turns-on the switch. The switch turn-on noise, therefore, is hidden in the horizontal blanking period at the far left of the monitor display.

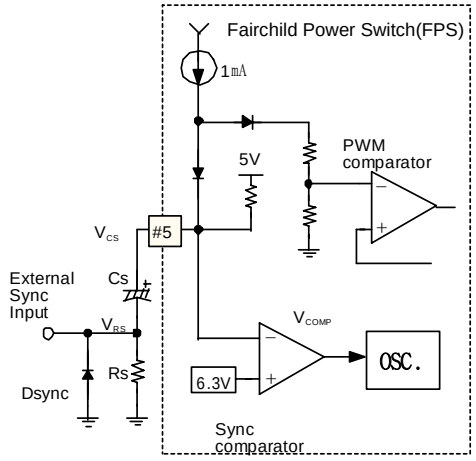


Figure 7. Synchronization circuit

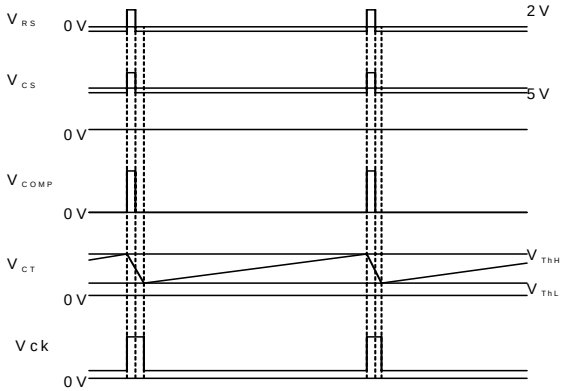


Figure 8. Synchronization circuit operation

2. Fairchild Power Switch (FPS) Built-In Protection Circuits

Since a Fairchild Power Switch's built-in protection circuits do not require additional external components, reliability is increased without increasing cost. Note that the protective circuitry can completely stop the SMPS operation (latch mode protection) until the power is turned off and on again. It can force the control voltage to restart above the ULVO level should the latch be released below ULVO (Auto Restart Mode protection).

2.1 Output Overload Protection

An overload is any load greater than the load defined as normal for operation. This is not a short circuit. The Fairchild Power Switch (FPS) overload protection determines whether the overload is true or merely transient. Only a true overload triggers the overload protection. When the Fairchild Power Switch (FPS) senses an overload, it waits for a specified time. If the overload is still present after this, it is considered a true overload and the device shuts down.

The Fairchild Power Switch (FPS) has a current control that prohibits current flow above a set maximum, which means the maximum input power is limited at any given voltage. Therefore, if the output load tries to draw more than this level, V_o (Figure 9) drops below the set voltage and LM431 can draw only a given minimum current. As a result, the opto coupler secondary current drops to almost zero. Almost the entire current flow at the node is from the Fairchild Power Switch (FPS) 1mA current source. Hence, the internal 3kΩ resistor (2.5R + R = 3KΩ) moves V_{fb} to 3V. From this point on, however, the 5µA current source starts to charge C_{fb} and, because the opto coupler secondary current is almost zero, V_{fb} continues to increase. When V_{fb} reaches 7.5V, the Fairchild Power Switch (FPS) shuts down.

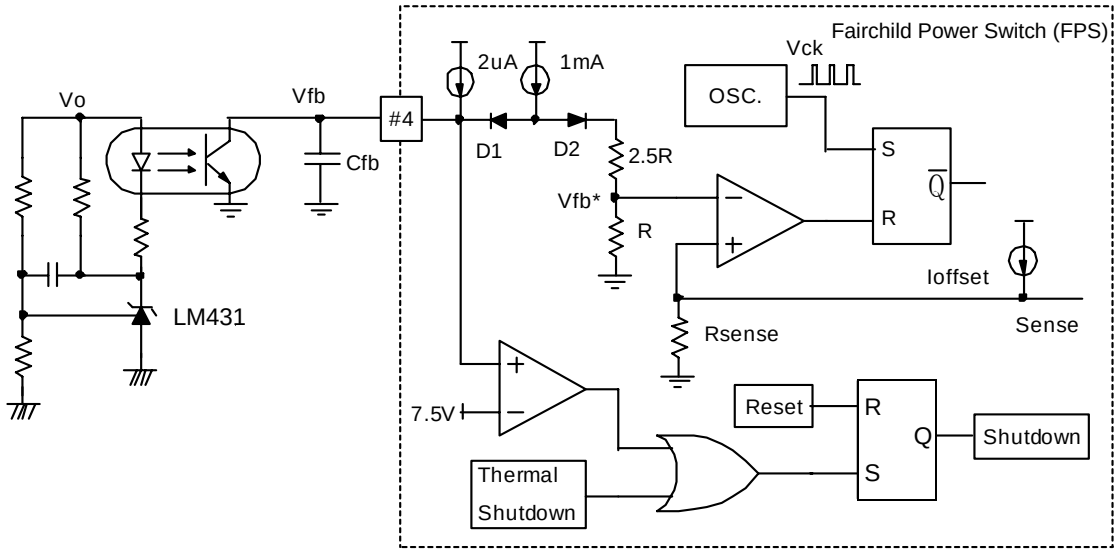


Figure 9. Fairchild Power Switch (FPS) overload protection circuit

The shutdown delay interval is therefore determined by C_{fb}. When C_{fb} is 10nF, the shutdown delay t2 (see Figure 10b) is about 9mS. With C_{fb} at 0.1µF, t2 is about 90ms. Such delay intervals do not allow the typical transients observed to shut down the Fairchild Power Switch (FPS). If a longer delay is needed, C_{fb} cannot be made arbitrarily large because it is important in determining the dynamic response of the SMPS.

When a large value of C_{fb} is necessary, a series-connected capacitor and Zener diode can be connected across C_{fb}, as shown in Figure 10a. In this combination, when V_{fb} is below 3V, the low-valued C_{fb} allows the SMPS to have a good dynamic response. When V_{fb} is above 3.9V, the high-valued C_d extends the delay time to the desired shutdown point. Where transients are insignificant and good dynamic response is not required, eliminate C_d and the Zener, thereby eliminating the added costs.

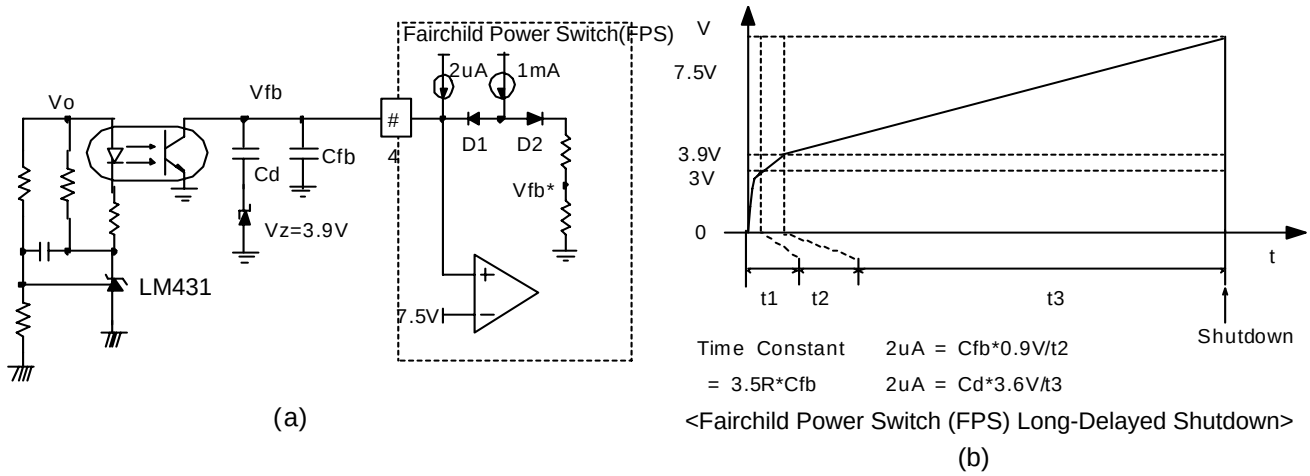


Figure 10. Long delay shutdown

2.2 Output Short Circuit Protection

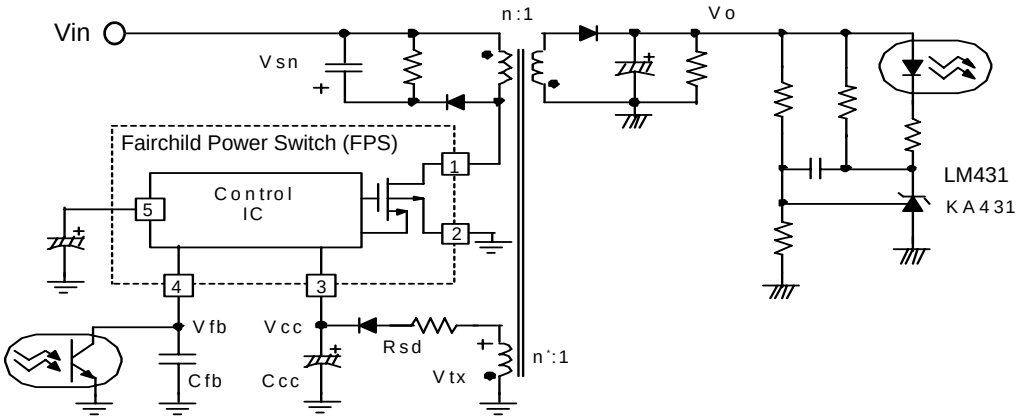
When the SMPS's output terminal is short circuited, the input current is at maximum. The output power however, is not a maximum because there can be no load voltage since the load is a short circuit. Under such conditions, the output short-circuit protection operates as follows:

When the output load short circuits a relatively large transformer winding in the SMPS, the Fairchild Power Switch's MOSFET current becomes much greater than I_{peak} because the inductor's magnetic core is unable to reset. This is due to low transformer coil voltage at turn off. This occurs because the current remaining in the inductor during the Fairchild Power Switch's minimum turn-on time cannot decrease by that amount during the remaining turn off time. Even though it is a large current, it does not unduly stress the MOSFET, but does greatly stress the transformer's secondary coils and the secondary-side rectifiers.

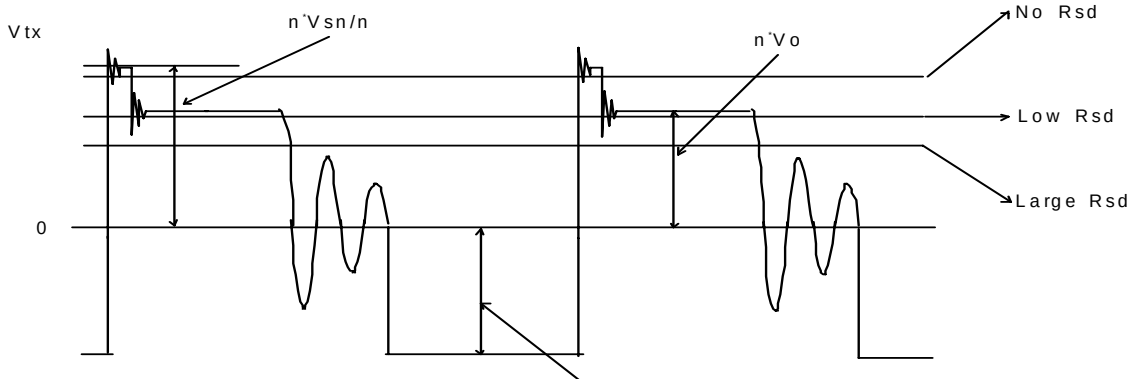
In most flyback or forward converters, the controller gets its power from a small secondary bias winding in the transformer. Furthermore, this controller voltage is proportional to the output voltage (see circuit of Figure 11a). This is fairly straightforward because, for a flyback converter, the coil voltage, when the switch turns off, is proportional to the output voltage.

For a forward converter, the transformer average voltage at turn off is proportional to the output voltage. For a flyback converter SMPS, the output short-circuit protection circuit can be operated in either latch mode or auto restart mode.

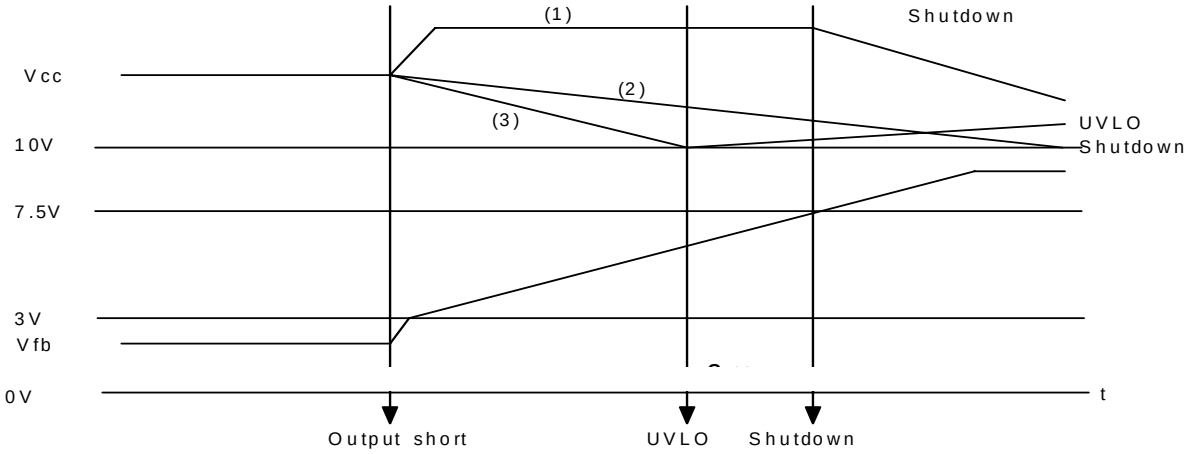
The change in V_{cc} as a function of Rsd is shown in Figure 11b. Rsd is shown in Figure 11a. When R_{sd} is zero, V_{cc} reaches the maximum value of V_{tx} (see lower primary winding, Figure 11a), i.e., $n'V_{sn}/n$, which is proportional to the maximum transformer current. For this case, if the output short circuits, V_{cc} increases and, after a specified delay, the protection circuit operates, entering the latch mode. However, when R_{sd} is made sufficiently large, V_{cc} can become smaller than $n'V_o$. Therefore, if the output short circuits, V_{cc} drops; but, if C_{cc} (see Figure 11a) is sufficiently large, V_{cc} stays at a level higher than the UVLO's lower threshold voltage (10V) until V_{fb} reaches 7.5V (Figure 11c-2) and latch mode protection starts. In contrast, if C_{cc} is small enough, V_{cc} approaches the UVLO's low threshold before V_{fb} reaches 7.5V (Figure 11c-3), and the UVLO operates instead of the protection circuit, stopping the device switching. In such a case, if V_{cc} exceeds the ULVO's upper threshold voltage (15V), auto restart operates again. R_{sd}, C_{cc}, and C_{fb} have effects even at start up and power down, so their values must be decided carefully. Experiments have indicated that 10-20W is most appropriate for R_{sd}.



(a) Flyback converter



(b) The voltage Vtx waveform of N_B and V_{CC} (the rectified V_{NB}), depending on Rsd



(c) Vcc and Vfb waveform's depending on the relative size of Cvcc at output short

Figure 11. Operation of the SMPS flyback converter's output short-circuit protection (latch mode)

2.3 Fast Protection Without Delay

As mentioned above, that the Fairchild Power Switch (FPS) shutdown capability is associated with a delay to allow normal transients to occur without shutting down the system. In effect, this restricts the protection range. If fast protection is required, additional circuitry is necessary. As shown in Figure 12, a transistor is used to force the feedback photodiode current to increase, causing the primary side V_{fb} to be forced below 0.3V. Therefore, the Fairchild Power Switch (FPS) stops switching. Depending on the magnitude of the photodiode current, the protection can be made to operate sufficiently fast. In such a case, when the transistor is turned off, the protection shifts to auto restart mode for normal operation. It is also possible to use this circuit as an output-enable circuit. Fast latch-mode protection can be implemented by adding a photocoupler. Thus, when the output terminal latch-mode transistor turns on, a large current flows through the photodiode PC2. A large current therefore flows through the primary phototransistor, which increases V_{fb} rapidly. This executes fast latch-mode protection with no time delay.

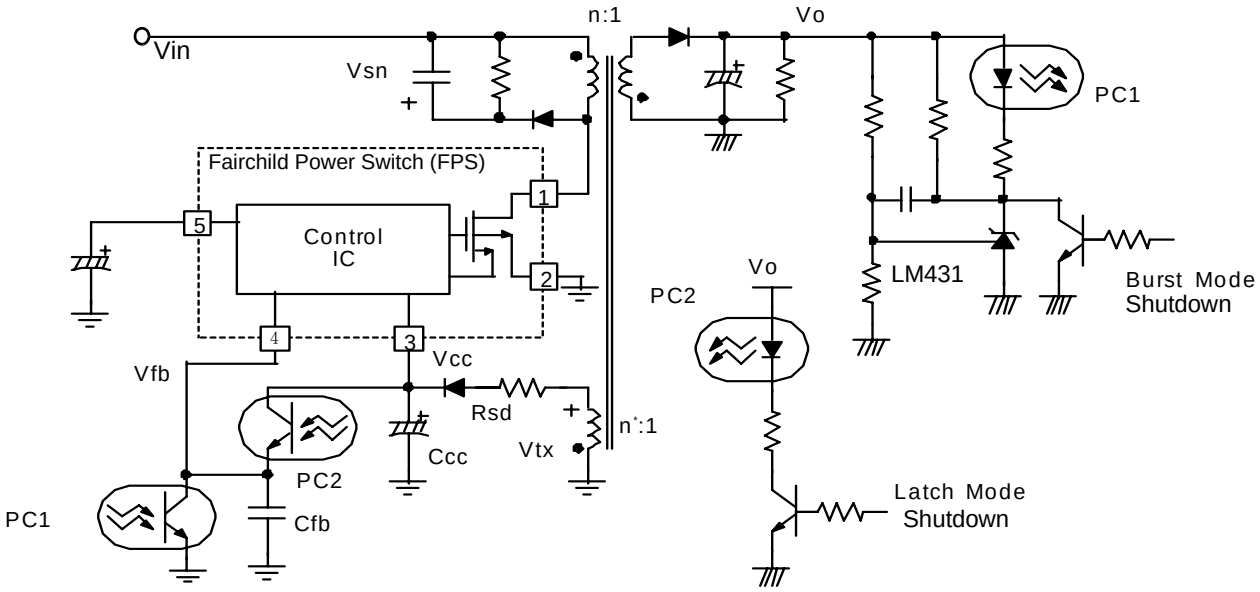


Figure 12. A fast protection circuit without a shutdown delay

2.4 Over-voltage Protection

The Fairchild Power Switch (FPS) has a self-protection feature that operates even when faults exist in the feedback path. These could include an open or short circuit. On the primary side, if the feedback terminal is short circuited, the voltage on it is zero and the Fairchild Power Switch (FPS) is unable to start switching.

If the feedback path open circuits, the protection circuit operates as though a secondary overload is present. Further, if the feedback terminal looks open due to some fault in the primary feedback circuit, the primary side could switch at the set maximum current level until the protection circuit operates. This causes the secondary voltage to become much greater than the rated voltage. In such a case, if there were no protection circuit, the fuse could blow or, more serious, a fire could start. It is possible that, without a regulator, devices directly connected to the secondary output could be destroyed. Instead, however, the Fairchild Power Switch (FPS) over-voltage protection circuit operates. Since V_{CC} is proportional to the output, in an over-voltage situation it also increases. In the Fairchild Power Switch (FPS), the protection circuit operates when V_{cc} exceeds 25V; therefore, in normal operation, V_{cc} must be set below 25V.

3. Noise Considerations at Switch Turn On

3.1 SMPS Current Sensing

Whether an SMPS is current-mode or voltage-mode controlled, or uses some form of non-linear control, it requires the protection afforded by current-sensing capabilities. Even though most current sensing uses a sensing resistor or a current transformer, there are instances where a MOSFET is used by the SMPS to further reduce current sensing losses. The Fairchild Power Switch (FPS) switching element is a SenseFET. This minimizes any power losses in the sense resistor, which is integrated onto the controller chip.

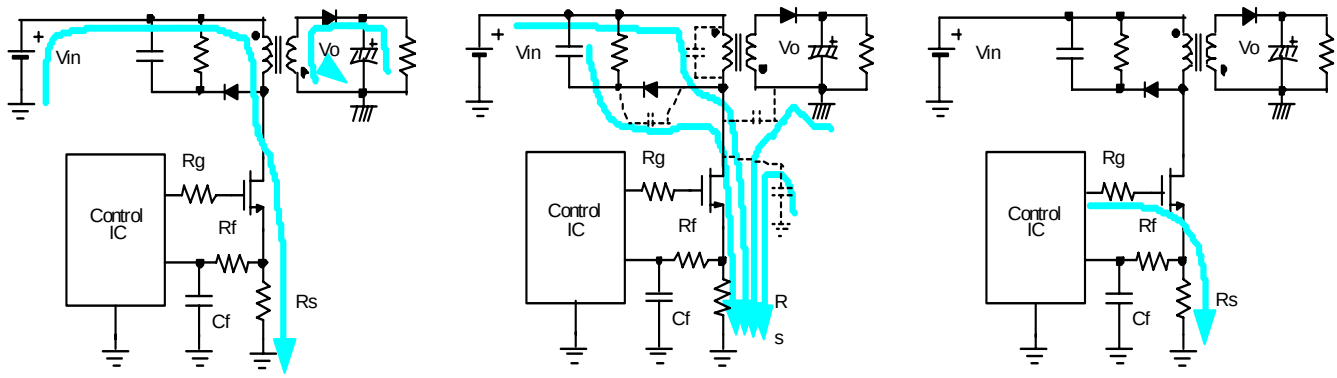
3.2 Current Sensing Waveform Noise After Turn On

A leading edge spike is present on the current sense line when the SMPS switching device turns on. It arises from three causes, as shown in Figure 13: (1) reverse recovery current; (2) charge/discharge current of the MOSFET shunt capacitance; and (3) MOSFET gate-operating current.

1. Reverse recovery current is generated when the SMPS operates in continuous-conduction mode (CCM; see Section 4.1). If the MOSFET is turned on while the rectifier diode is conducting, the diode, during its reverse recovery time, acts like a short circuit; therefore, a large current spike flows in the MOSFET. There are three ways to reduce the magnitude of this (reverse recovery) current: use a fast recovery diode; reduce the MOSFET's gate-operating current at turn on; or, increase the transformer leakage inductance.

2. The total capacitance on the MOSFET's drain side includes the parasitic capacitor C_{ds} between the drain and the source terminals, the junction capacitance of the snubber diode, and the capacitance of the transformer windings. At turn on, the total equivalent capacitor discharges through the MOSFET.

3. As shown in Figure 13, the MOSFET gate-operating current also flows through the current-sensing resistor.



Reverse Recovery Current

Charge/Discharge Current of the Equivalent Capacitor

MOSFET Gate Operating Current

Figure 13. Current sensing waveform noise after turn on

3.3 Dealing With Leading Edge Noise

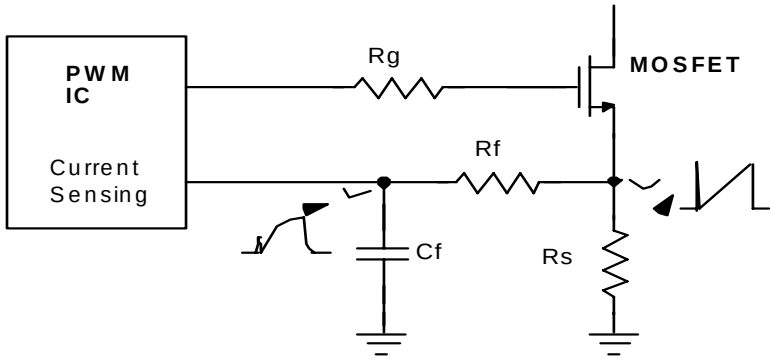
Among the measures taken to reduce leading edge noise, the most commonly used technique is the RC filter. As shown in Figure 14a, the RC filter is effective against the noise, but its disadvantage is that it distorts the current sensing signal so that accurate current sensing becomes difficult.

Furthermore, a large RC value may be difficult to implement on an IC and may even require a bigger chip. The technique of leading edge blanking (LEB), as presented in Figure 14b and 14c, overcomes the distortion disadvantage of the RC technique. Since the problem noise arises just after turn on, if a circuit is inserted that ignores the current sensing line for a fixed time just after turn on, operation can continue normally regardless of the noise. Whatever the details of the location and type of circuit used, the basic idea is to maintain a minimum turn-on time; to use the shortest turn-on time that cannot be terminated once turn-on starts. Duty ratio control with a minimum turn-on time is implemented through a non-linear control method with a very wide control range relative to a linear control. The non-linear control operates such that if load conditions require a turn-on time of 400ns when the minimum turn-on time is set at 500ns, one switching cycle turns on at 800ns. The next cycle is missed, ensuring that the average turn-on time is 400ns. In this case, every other cycle is missed. This is pulse skipping. In this case, the switching frequency will be half that of a linearly controlled system, thereby improving SMPS efficiency at light loads. The input power is therefore minimized. The Fairchild KA34063 DC/DC converter is an example of a non-linear control IC.

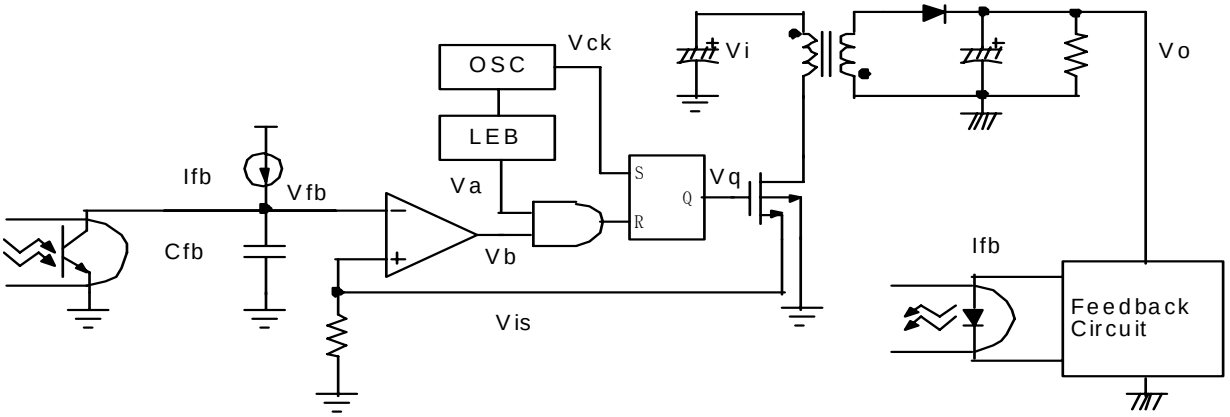
3.3.1 Burst-Mode Operation

The aforementioned method can be viewed as an example of burst mode operation. Burst-mode operation, by reducing the switching frequency, is one of the most useful ways to improve SMPS efficiency at light loads and to reduce the standby input power of household appliances. Note that burst-mode operation is not a burst oscillation (as in ringing choke conversion circuits), which can bring about reliability problems. There are mainly two types of true burst-mode operation: one type lowers the switching frequency equally; the other switches at normal frequency for a fixed time and stops the control IC operation for a large number of cycles. Even though, in the first method, the control IC continues to consume power, the output voltage ripple is minimized.

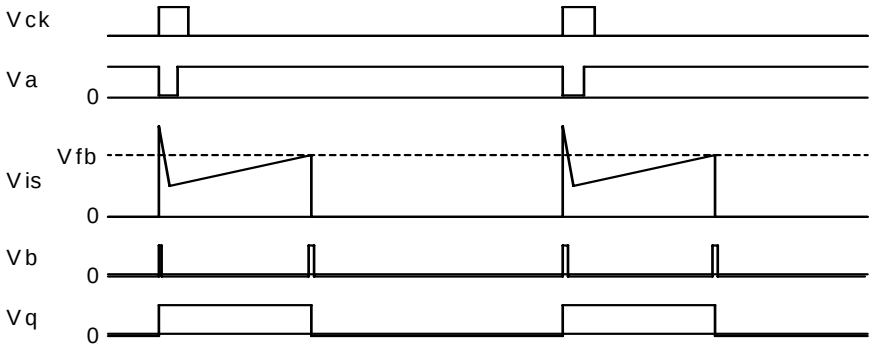
The second method can be a useful way to reduce the minimum input power at standby (since the standby power is greatly reduced when the IC is stopped). Indeed, it is often used in cell phones to reduce the DC/DC converter’s power consumption in standby mode. However, it has the disadvantage of a larger output voltage ripple. Currently, Europe restricts household appliance standby input power to less than 5W and, in time, it will be required to be less than 3W. For such needs, burst mode operation is a powerful method to satisfy the requirement for reduced standby input power.



(a) Noise elimination using RC filter



(b) Internal block diagram for noise elimination using LEB



(c) Noise elimination and waveforms in LEB

Figure 14. Leading edge blanking

4. Flyback Converter Operation

4.1 Operation In Continuous Conduction Mode (CCM)

Figure 15 shows a typical flyback converter. When the current through the converter's inductor is always greater than zero within a switching cycle, the converter is said to be operating in the continuous conduction mode (CCM). Figure 16 shows the waveforms of CCM operation, which operates as follows.

4.1.1 For $t_0 \sim t_1 = T_{ON}$

At t_0, the MOSFET turns on. Immediately before t_0, the inductor current is flowing through diode D, but when the MOSFET turns on, D turns off, thereby isolating the output terminal from the input terminal. At MOSFET turn on, its V_{DS} goes to zero and V_D becomes (V_o + V_i/n). During the interval after MOSFET turn on (i.e., from t_0 on), V_i is applied to L_m, so I_{Lm} increases linearly with a slope, as shown by the following equation:

$$\text{Slope} = \frac{V_i}{L_m} \tag{1}$$

When the energy flow is examined, it appears that the input power source supplies energy to L_m while the MOSFET is on. However, since the energy in L_m continues to increase while the output terminal is isolated from the input terminal, it is C_o that has to supply the output current during this interval.

4.1.2 For $t_1 \sim t_2 = T_{OFF}$

At t_1, the MOSFET turns off. At the instant of turn off, the inductor current that flows through the MOSFET starts to flow through diode D. When D turns on, V_{DS} becomes (V_i+nV_o). During this interval, the voltage nV_o is applied to L_m so that I_{Lm} decreases in a straight line with the following slope:

$$\text{Slope} = \frac{nV_O}{L_m} \tag{2}$$

When the energy flow during this interval is examined, it appears that the inductor energy is delivered to the output. The energy in L_m is reduced by the amount of energy it delivers to the output. When the MOSFET turns on again, at t_2, one switching cycle ends.

4.1.3 Relationship Between Input and Output

As shown in Figure 16, the colored areas A and B of the waveform V_{Lm} (the voltage applied to the inductor) must be equal because the average voltage of the inductor or transformer in steady state is always zero. Therefore:

$$V_i T_{ON} = nV_O T_{OFF} \tag{3}$$

$$\frac{nV_O}{V_i} = \frac{T_{ON}}{T_{OFF}} = \frac{D}{1-D} \tag{4}$$

the input and output currents become:

$$I_i = DI_{Lm,\,AVG} \tag{5}$$

$$I_O = n(1-D)I_{Lm,\,AVG} \tag{6}$$

hence the input and output powers are equal. An ideal waveform is shown here because the effect of leakage inductance has been ignored. In reality, leakage inductance causes ringing.

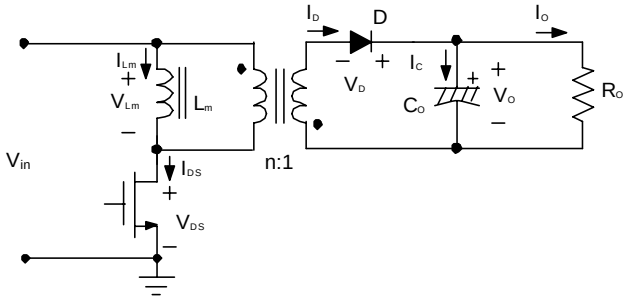


Figure 15. A typical flyback converter

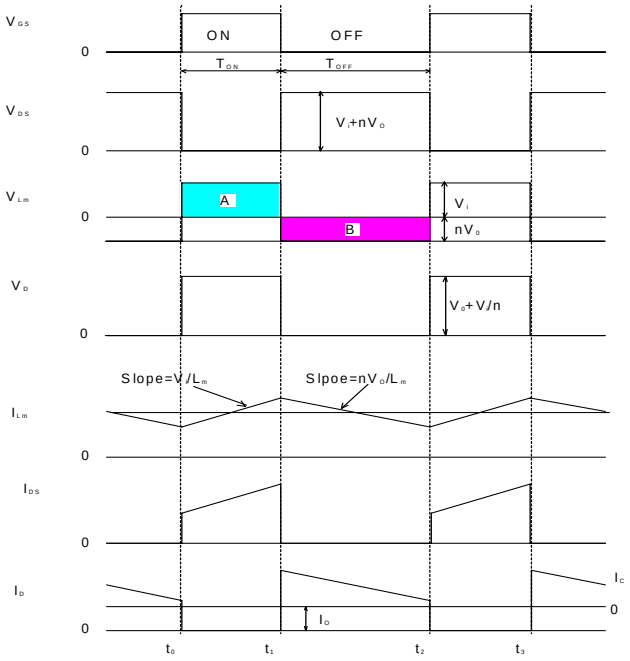


Figure 16. Flyback converter operating waveforms in continuous current mode (CCM)

4.2 Discontinuous Conduction Mode (DCM)

The appearance of an interval in which the inductor current becomes zero during a switching cycle marks flyback converter operation as discontinuous conduction mode (DCM). As shown in Figure 17, the voltage waveform applied to the inductor, V_{Lm}, becomes more complex in DCM. To avoid difficulties in computation, T_{OFF} is not used. Instead, three input and output relationships of a converter are derived using T_{OFF}* the time when the output rectifier diode is actually conducting.

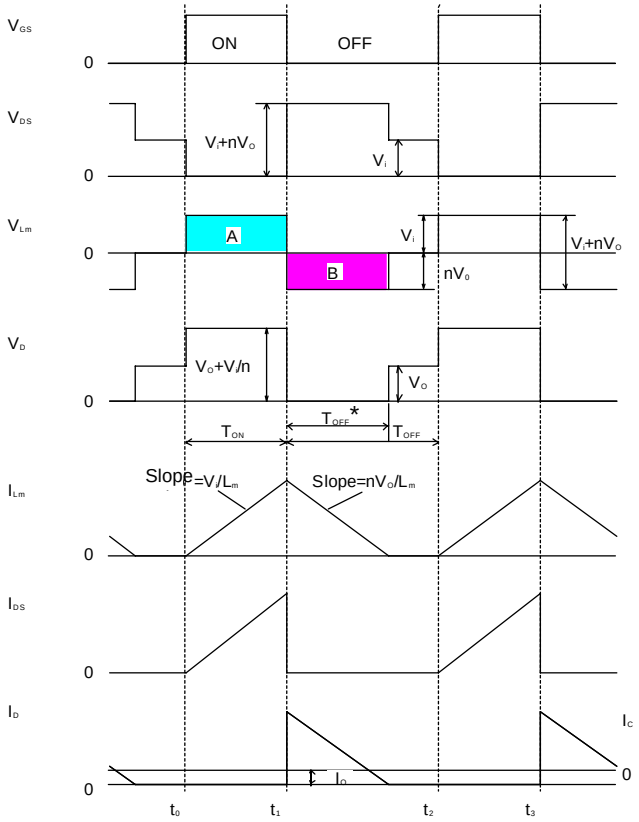


Figure 17. Flyback converter operating waveforms in discontinuous current mode (DCM)

The boundary condition between DCM and CCM is:

$$I_i + I_O = \frac{V_i}{2L_m} T_{ON} \quad (7)$$

The following input-output relationship in DCM is derived using the fact that the colored areas A and B of V_{Lm} in Figure 17 must always be equal because, in steady state, the average inductor (or transformer) voltage is always zero.

.

$$V_i T_{ON} = nV_O T^*_{OFF} \quad (8)$$

$$\frac{V_O}{V_i} = \frac{T_{ON}}{T^*_{OFF}} = \frac{D^*}{1-D^*} \quad (9)$$

Deriving the above equation again, using I_o and the fact that the input and output powers are equal, V_o is obtained as:

$$V_O = \frac{(V_i T_{ON})^2}{2\frac{I_O}{n} L_m (T_{ON} + T_{OFF}) + V_i} \quad (10)$$

The following equation represents the input power:

$$P_{IN} = \frac{1}{2} L_m I^2_{Lm,(peak)} fsw \quad (11)$$

where f_{sw} is the switching frequency.

4.3 Flyback Converter Design

4.3.1 Turns Ratio Considerations

The turns ratio of an SMPS's flyback converter transformer is an important variable. It affects the voltage and current levels associated with the primary-side switching device and the secondary-side rectifier, as well as the number of turns on the transformer and the current through it. A frequently discussed design concept suggests operating at maximum duty ratio when the input voltage is a minimum. For simplified calculations, assume that operating conditions change as listed below:

- V_{ac} input: 85 ~ 265V_{ac}

- V_{dc} (rectified voltage): 100 ~ 400V_{dc}

- Output voltage: 50V_{dc}

- Inductor current: Continuous conduction mode (CCM) operation assumed.

The input power taken by the DC source is the product of the DC voltage and average input current. Using a wide duty cycle to deliver equal average current reduces efficiency. A narrow duty cycle increases the effective current on the primary side, increasing the operating temperature of the primary winding and the MOSFET. It is best to decide on a turns ratio, n, based on the device used. If the voltage on the primary side MOSFET is relatively low (e.g., 600V), make *n* small; if it is on the high side (e.g., 800V), make n large. As the value of n increases, the primary side switching device current and the secondary-side rectifier diode voltage decreases. Hence, with high output voltage and multiple secondary side outputs, it is advantageous to increase *n*.

4.3.2 Deciding the Operating Current Mode

As discussed in Sections 4.1 and 4.2, there are two different operating current modes possible in a flyback converter: the continuous conduction mode (CCM), and the discontinuous conduction mode (DCM). The advantages and disadvantages of each are reviewed below to help the designer make the best choice.

4.3.2.1 Characteristics of the Discontinuous Conduction Mode

In a flyback converter design, if discontinuous conduction occurs just at minimum input voltage and maximum output power, discontinuous conduction must be considered to be the case for all input conditions. The flyback converter's input power in discontinuous conduction mode can be expressed as:

$$P_I = \frac{1}{2} L_m I_P^2 f_{sw} \quad (12)$$

Regardless of any changes in input voltage, the power equation indicates that the input current is limited by the peak value of the current flowing through the MOSFET in the transformer primary. A Fairchild Power Switch (FPS) has an integrated over-current protection feature (see Section 2.1, above). This feature does not require external components and operates across the range of input current. However, the fixed-operating current of DCM, tends somewhat to offset the effect of the larger effective primary-side current. The gain is at the low-frequency end where core loss is not a problem since only a minimum number of turns need be wound. Also, turn-on loss is not a serious problem due to the low input current. Other losses; such as eddy current, skin effect, proximity effect, etc., are not significant. A more clearly defined advantage of DCM operation is that it permits the use of a slow, low-cost secondary rectifier diode. In contrast to the continuous conduction mode, in the discontinuous conduction mode, the effective current is higher, requiring the use of heavier wire and thicker coils. Therefore, DCM does not bring an advantage insofar as transformer construction is concerned. Moreover, DCM causes the MOSFET operating temperature to increase because of the large effective primary-side current, as described in Section 4.3.1.

4.3.2.2 Characteristics of the Continuous Conduction Mode

Since the coils' effective current is decreased, CCM brings the advantage of lighter wire. The smaller effective current also reduces MOSFET heating. This is a definite advantage for average input current. On the other hand, CCM operation requires consideration of the rectifier diode's reverse recovery current. Depending on the diode's reverse recovery time (t_{rr}), the reverse recovery current may stress the diode and increase the loss at its end terminals. It is therefore necessary to use a diode with the minimum t_{rr} possible within the allowable cost range.

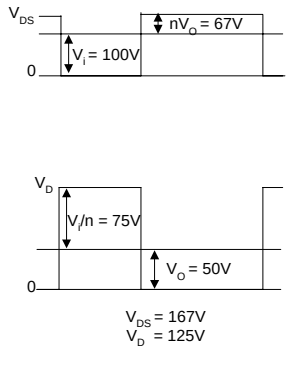
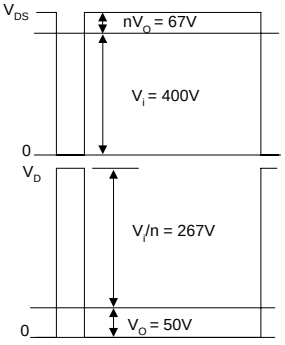
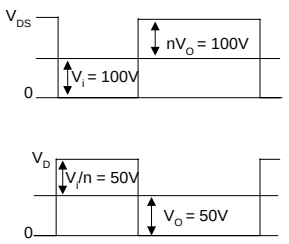
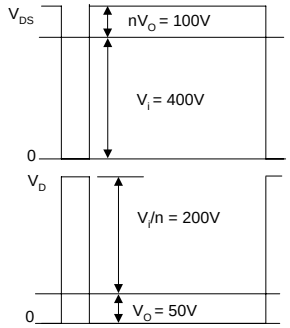
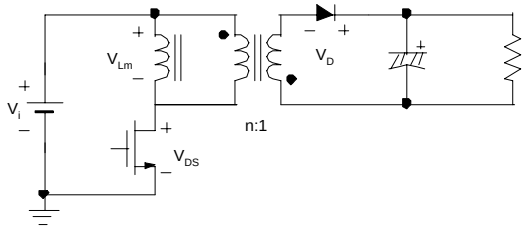
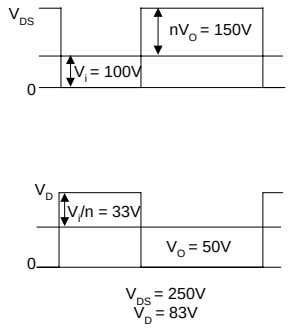
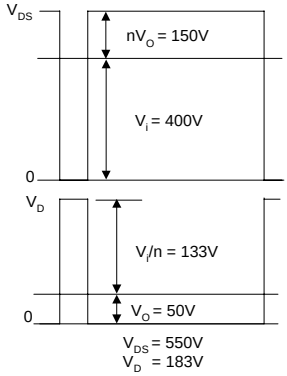
n	Vi = 100V	Vi = 400V	Merits & demerits
1	 V_{DS} = 167V V_D = 125V	 V_{DS} = 467V V_D = 317V	■ Voltage applied to switch device is low ■ Effective current in switching device and primary winding is low ■ Voltage applied to rectifier diode is high ■ Output voltage ripple is small ■ Control must be done through short turn-on time
	 V_{DS} = 200V V_D = 100V	 V_{DS} = 500V V_D = 250V	 ■ Intermediate Design Method
	 V_{DS} = 250V V_D = 83V	 V_{DS} = 550V V_D = 183V	■ Voltage applied to switch device is high ■ Effective current in switching device and primary winding is high ■ Voltage applied to rectifier diode is low ■ Output voltage ripple is large ■ Control must be done through long turn-on time

Figure 18. The current and voltage ratings required on the primary-side switching device and the secondary-side rectifier diode depend on the turns ratio (*n*) selected

4.3.2.3 Designer's Choice

As is clear from the above discussion, DCM operation can be advantageous in cost and efficiency, if the input is small and it is required to precisely control the input power through the primary side switch (MOSFET) current.

On the other hand, for large inputs and where switching turn on loss could be a major problem, a CCM design would be more advantageous. In conclusion, the system designer must decide between the two modes to best fit the characteristics of the system being designed.

5. The Transformer

5.1 Why a Transformer is Needed

There are three reasons for needing a transformer in a power conversion circuit. The first reason is safety. A transformer affords electrical isolation between the primary and secondary sides, as shown in Figure 19a. In addition, a true ground on the output side helps prevent electric shock. The second reason is for voltage conversion. For example, if a DC/DC converter (such as the buck converter shown in Figure 19b) switching at 50kHz is used to obtain 5V from 100V, the duty cycle would only be 5%. Using a 50kHz switching frequency, the control circuit may have only about 1μs to act, which is not an easy task. Even if this were possible, the internal voltage and current for each element would be very large, reducing efficiency. The problem is aggravated at high output current. In the above example, using a transformer to lower the voltage to 10V would allow an on time of about 10μs. This is strategy lowers cost and raises efficiency. The third reason to use a transformer has to do with high voltages and voltage fluctuations. For example, even though all control for a 1000V supply is handled by the 5V power source on the GND side, a transformer is necessary if power is needed for current sensing at the 1000V output terminal or for other control. If the isolation voltage between the transformer windings is sufficient, a 1000V potential difference can be safely maintained between the primary and secondary windings and power can be delivered. Further, a transformer is also required when the power GND has a sudden potential fluctuation, as in a half-bridge converter, gate drive power source.

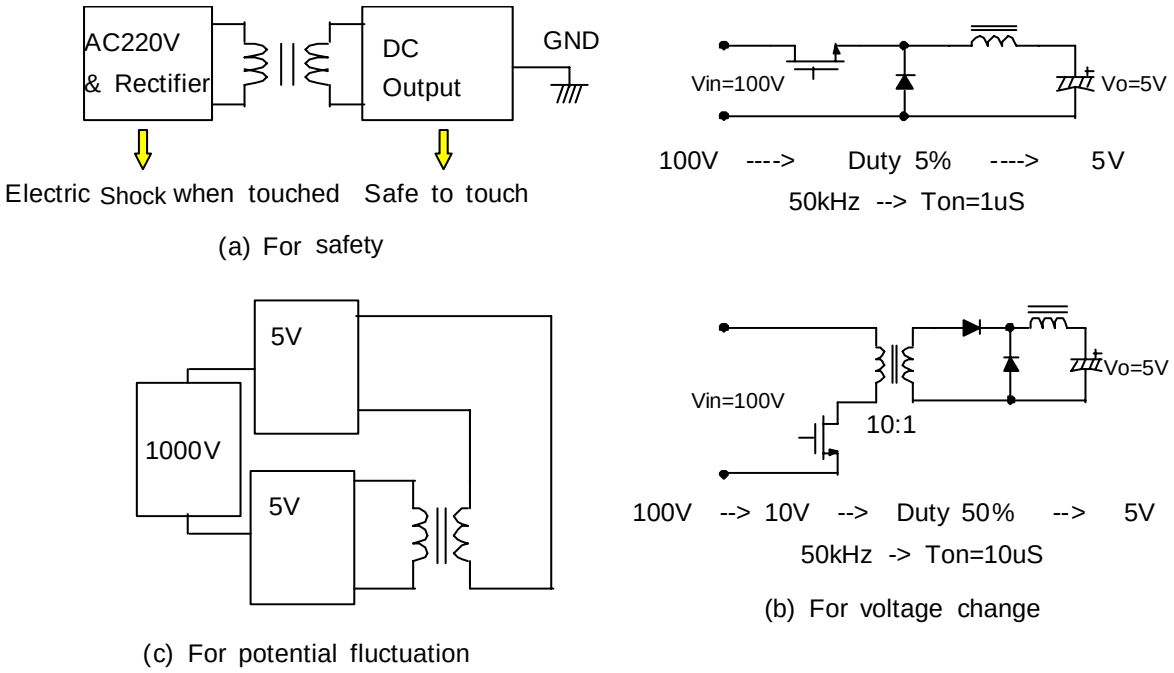


Figure 19. Why a transformer is needed

5.2 The Ideal Transformer

The transformer is a device that uses inductive coupling between its windings to deliver power or signals from one winding to the another. This is usually from the primary winding to the secondary winding. The voltages across the windings can be raised or lowered with respect to each other and, if necessary, the primary and secondary sides can be isolated from each other. Figure 20 shows an ideal transformer, a simplistic model useful in describing the transformer concept. An ideal transformer which is actually a fictional concept that must satisfy the following three conditions:

1.The coupling coefficient between the windings is unity (i.e., the leakage flux is zero).

2.The coil loss is zero (the device has no losses).

3.The inductance of each coil is infinite.

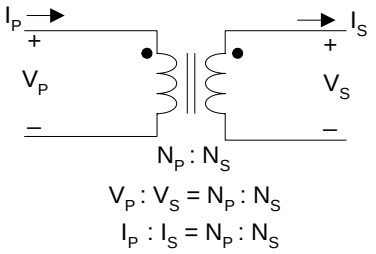


Figure 20. Ideal transformer

The input-to-output voltage ratio of an ideal transformer is directly proportional to the turns ratio. This is the ratio of the number of turns on the primary winding to the number of turns on the secondary. The polarity is represented schematically by the placement of a dot on each winding. Since n= V_p/V_s, and an ideal transformer has no loss, the current ratio is inversely proportional to the turns ratio. The current direction is such that it enters on one side and leaves on another. Thus the sum of all the nI that flow into the dot is zero. The dot, indicating the winding polarity, is placed to make the flux direction in the transformer core uniform when current flows into the dot. Furthermore, in the case of an ideal transformer, if the path on the secondary side windings is opened, there is no secondary current flow and the current on the primary side also goes to zero.

5.3 The Real Transformer

Significant differences exist between an ideal transformer and a real one. In a real transformer:

1. The coupling coefficient between each coil is finite and, when a gap is placed in the core as is done in many power transformers, the coupling coefficient becomes still smaller (i.e., there is leakage flux);
2. There are losses, such as iron (hysteresis) loss, eddy current loss, coil resistance loss, etc.; and,
3. The inductance of each coil is finite. When a gap is placed in the core, the inductance becomes still smaller.

In a real transformer, should the secondary side be opened current continues to flow in the primary. While energy cannot be stored in the ideal transformer, it is stored in a real transformer. The so-called magnetizing inductance accounts for this energy storage phenomenon. The circuit of Figure 21 is a simplistic view of an actual transformer and shows the magnetizing inductance. Figure 22 presents a more complete equivalent circuit of a real transformer, showing inductances and loss resistances.

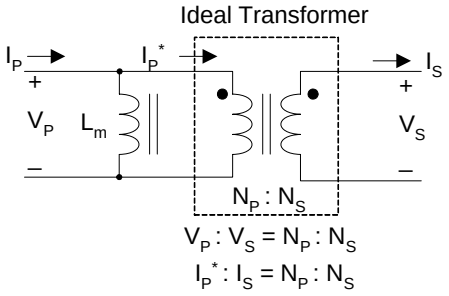
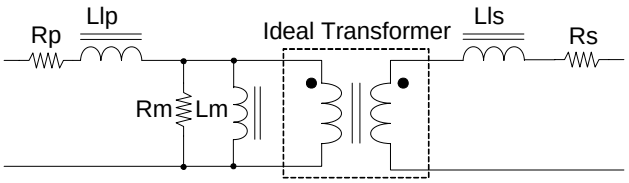


Figure 21. A model of an actual transformer showing the magnetizing inductance L_m, which accounts for energy storage



-. Rp: Primary side winding resistance
-. Rs: Secondary side winding resistance
-. Llp: Primary side leakage inductance
-. Lls: Secondary side leakage inductance
-. Lm: Magnetizing inductance
-. Rm: Transformer core loss resistance

Figure 22. A more complete equivalent circuit of an actual transformer, showing inductances and loss resistances

6. Transformer Design

6.1 Core Selection

The maximum power that a transformer core can deliver and the maximum energy a transformer inductor can store depends on the shape and size of the core. In general, as the effective cross sectional area (Ae) increases, more power can be delivered. Also, as the window area (Aw) on which the coils are wound increases, more and thicker windings can be used, allowing a further increase in the power that can be delivered. The product of Aw and Ae is called the area product, AP, and the maximum power a transformer can deliver is proportional to an exponential power of AP. Recent transformer theory shows designs depending almost entirely on AP. In the broader view, a flyback converter transformer can be viewed as a coupled inductor, so it's common to design a flyback transformer using inductor design methods. The two equations below, (13) and (15), represent two ways to calculate AP. Equation (13) based on whether or not the core is saturated, is appropriate at low operating frequencies. Equation (15), limited by core loss, is appropriate at high frequencies. For any given design, it is necessary to calculate AP using both equations. The equation that gives the higher value is the one that must be considered correct. Equation (13) assumes that all losses are wire losses and ignores the core (iron) loss.

$$AP = \left(\frac{LI_P I_{RMS} 10^4}{420 K B_{MAX}}\right)^{1.31} [cm^2] \qquad (13)$$

L = Inductance of Transformer
Ip = Operating peak current
Bmax = Maximum operating flux density
Irms = RMS current

L and B_{MAX} are in Henries and Tesla units, respectively, and K is listed in Table 1, below. From the above equation, the current density (J) per unit area of wire is obtained from the current by the relationship below, which assumes that the temperature of the inductor's "hot spot" is 30°C above ambient.

$$J_{30} = 420 AP^{-0.24} [A/cm^2] \qquad (14)$$

At any operating frequency high enough for the core losses to become large, the following equation (15) should be used. Specifically, it assumes that the total transformer losses are split equally (50/50) between the wire and the core.

$$AP = \left(\frac{L\Delta I_m I_{RMS} 10^4}{130K}\right)^{1.58} (K_H f_{SW} + K_E (f_{sw})^2)^{0.66} [cm^2] \qquad (15)$$

L = Inductance of Transformer
Ip = Operating peak current
Irms = RMS current

In equation (15), K_H is the hysteresis coefficient (typically 4 x 10^{-5} for ferrite cores) and K_E is the eddy current coefficient (typically 4 x 10^{-10} for ferrite cores).

The current density relationship, represented by the equation for J_{30} assumes a hot spot temperature of 15°C above ambient, with the iron loss adding on an additional 15°C (a total of 30°C above ambient).

$$J_{30} = 297 AP^{-0.24} [A/cm^2] \qquad (16)$$

The parameter K in equation (13) is the product of the window utilization factor K_U with the primary area factor K_P (see Table 1). K_U is the ratio of the cross sectional area of the winding's copper to the entire window area, and it is significant in setting the isolation between the primary and secondary sides. Because it is related to the transformer shape and winding method, the designer should know the value of K_U for the transformer usually used.

The value of K_U can vary greatly, depending particularly on how closely the isolation safety standards (re isolation) are followed; the K_U of Table 1 assumes a general bobbin is used. K_P is the ratio of the area of the primary winding to that of the total winding. In Table 1, it is unity for the inductors because a buck boost inductor has no secondary windings. For the flyback transformer coupled inductor, K_P is usually 0.5, as Table 1 shows. Such an inductor has the highest efficiency when the primary and secondary winding areas are equal. When there are more secondary windings, however, the K_P for a flyback transformer coupled inductor can be lower more than 0.5. Note that the ease and speed of obtaining an accurate AP from equations (13) and (15) depends on the designer's experience. A reasonably good knowledge of the probable values of the three parameters K_U, K_P, and J for the flyback transformer being designed reduces the number of trial and error attempts necessary.

Table 1. K_U, K_P, and *K*

	K_U	K_P	$K = K_U K_P$
CCM Buck, Boost Inductor	0.7	1.0	0.7
DCM Buck, Boost Inductor	0.7	1.0	0.7
CCM Flyback Transformer	0.4	0.5	0.2
DCM Flyback Transformer	0.4	0.5	0.2

6.2 Determining the Number of Turns

Although the equation for the minimum number of flyback transformer turns can be determined using applied voltage and maximum turn-on time, the equations used here are derived from the relationship between L and I_P.

For an AP determined from equation (13), above, calculate N_{MIN} using the following equation:

$$N_{MIN} = \frac{LI_P}{B_{MAX}A_C}10^4 \quad (17)$$

L = Inductance of Transformer
Ip = Operating peak current
B_{MAX} = Maximum operating flux density
Ae = Effective cross-sectional area of core

For an AP determined from equation (15), above, calculate N_{MIN} using the following equations:

$$N_{MIN} = \frac{L\Delta I_m}{\Delta B_m A_C}10^4 \quad (18)$$

L = Inductance of Transformer
Ip = Operating peak current
B_{MAX} = Maximum operating flux density
Ae = Effective cross-sectional area of core

6.3 The Windings

The cross-sectional area of the winding must be obtained from the calculated effective current and the current density (from the appropriate equation above), factoring in the number of turns (as determined from a calculation of NMIN). If eddy current loss is not a serious problem, divide the effective current by the current density, thereby determining the coil cross-sectional area. Be aware, however, that as the coil becomes thicker, the problem of eddy current loss arises. Using twisted thin coil strands (Litz wire), instead of a single heavy wire, can reduce the eddy current loss, but K_U becomes smaller.

6.4 Determining the Gap

It is not easy to precisely calculate the required gap; however, the gap can be calculated from the following equation. It is based on the fringing effect of the surrounding flux. Note that the calculated value of L is usually larger than required;

$$l_g = \frac{u_O u_r N^2 A_C}{L}10^{-2}[cm] \quad (19)$$

U_O = Permeability of free space
U_r = Relative permeability

therefore, the gap must be changed to obtain the required value of L.

References

1. *Transformer and Inductor Design Handbook.* 2nd ed. Col. Wm. T. McLyman. Marcel Dekker, Inc., 1988.

2. *Switch Mode Power Supply Handbook.* Keith H. Billings. McGraw-Hill, Inc., 1989.